Design and Fabrication of Millimeter-Wave GaN HEMTs

Keisuke Shinohara, Dean Regan, Casey King, Eric Regan, Petra Rowell, Andrea Arias, Andrew Carter, Joshua Bergman, Miguel Urteaga, Berinder Brar
Teledyne Scientific Company

Teledyne Scientific Company, 1049 Camino Dos Rios, Thousand Oaks, CA 91360,
Keisuke.Shinohara@Teledyne.com, +1-805-373-4049

Keywords: GaN HEMT, Millimeter-wave, transistor scaling, current collapse, BRIDGE HEMT, thermal resistance, micro-device cell array

Abstract

In this paper, we describe design and fabrication of millimeter-wave GaN HEMTs. We present unique design approaches to improve device frequency performance, efficiency, output power, and linearity, while addressing issues related to thermal management, reliability, and manufacturability.

INTRODUCTION

Next-generation millimeter-wave RF systems require higher efficiency, output power, linearity, and wider bandwidth. However, these parameters are in a trade-off relationship that becomes more prominent as operational frequencies increase due to the narrower design window and increased parasitic effects on the frequency performance for millimeter-wave transistors, as compared to microwave transistors. In this paper, we present GaN HEMT technologies that address three technical areas: (i) epitaxial and gate designs for deeply-scaled AlGaN/GaN HEMTs targeting W-band applications, (ii) multiple 2DEG channel HEMT designs for RF switch and linear power amplifier (PA) applications, and (iii) micro-scale device cell concept for device-level thermal management.

GAN-HEMT SCALING FOR W-BAND APPLICATIONS

As the frequency of operation increases, the dimension of the device, including epitaxial layer thicknesses, source-to-drain distance (L_{sd}), gate length (L_g), field plate length, and dielectric thicknesses of the field plate(s), must be proportionally reduced by 1/frequency to maintain proper electrostatics. In addition, parasitic resistances and capacitances, including gate fringing capacitances, have a more significant impact on the frequency performance of the transistors, thus limiting their gain and efficiency, especially at W-band frequencies and above. The reduction in size and increase in parasitic effects constrain the device design window as well as the fabrication process window, thereby making it harder to co-optimize frequency, output power, and efficiency performance. In this section, we present our design and fabrication of high-frequency GaN-HEMTs targeting low-noise and PA applications at W-band frequencies.

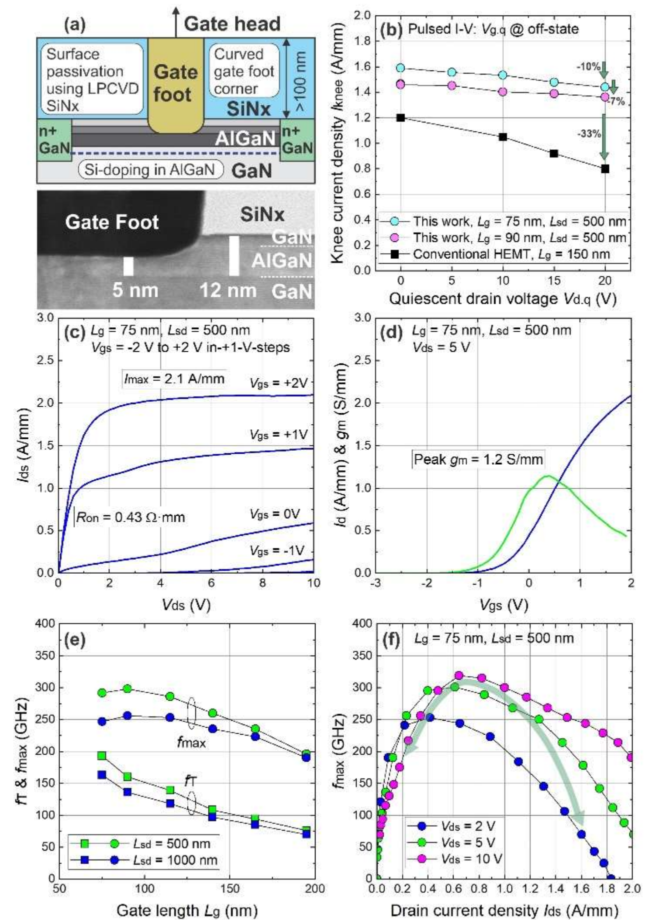

Fig. 1. Technology cross-section of our deeply-scaled AlGaN/GaN HEMT and a cross-sectional TEM image of the gate foot (a). Knee current densities as a function of a quiescent drain voltage, at an off-state $V_{g.q} = V_{th} - 2V$ (b). Output (c) and transfer (d) characteristics of a 75-nm-gate HEMT. Measured f_T and f_{max} as a function of the gate length (e). f_{max} as a function of drain current density (f).

Fig. 1(a) illustrates a cross-section of deeply-scaled GaN HEMT technology designed for W-band applications. The epitaxial structure consists of a GaN cap, an AlGaN barrier, and a GaN channel layer. The total thickness of the GaN cap

and AlGaN barrier layers is 12 nm, where the AlGaN barrier thickness under the gate foot is reduced to 5 nm through gate recess etching using low-power RIE, to maintain a high gate-to-channel aspect ratio of >10 (L_g/d, where d is the gate-to-channel distance) for short L_g of >50 nm. The AlGaN barrier layer is doped with Si to achieve two goals: (i) passivating donor-like trap states that exist at the GaN-on-AlGaN interface [1] to reduce electron trapping effects, and (ii) increasing the 2DEG density (n_s) in the GaN channel through the modulation doping to increase transistor current density. The measured n_s and electron mobility are 1.3×10^{13} cm^{-2} and 1900 cm^2/V·s, respectively. The n+GaN ohmic contacts are formed using MBE regrowth, with a low access resistance (R_{ac}) of 0.1 Ω·mm from an ohmic metal to the n+GaN/2DEG interface. Another key feature is the gate foot with round corners (Fig. 1(a)) formed through gate recess RIE process optimization, which helps alleviate the electric field under large signal operation. The combination of the epitaxial design and the gate structure enables greatly reduced knee current collapse, <10% at a quiescent drain voltage of 20V, compared to our conventional 150-nm T-gate GaN HEMTs, without requiring an additional field plate structure (Fig. 1(b)). The 75-nm-gate device, with a L_{sd} of 500 nm, exhibits a maximum drain current density exceeding 2 A/mm, with an on-resistance (R_{on}) of 0.43 Ω·mm and a peak g_m of 1.2 S/mm (Fig. 1(c), (d)). Measured f_T and f_{max} exhibit good scaling behavior with L_g, while the devices with a longer L_{sd} of 1000 nm show an increased parasitic effect at shorter L_g <140 nm (Fig. 1(e)). The 75-nm-gate device also exhibits high power gain (f_{max}) in the broad I_{ds} range along the load line, with a peak value of 320 GHz at around class-AB bias conditions (Fig. 1(f)). These device characteristics are important in low-noise and power amplifiers at W-band frequencies. The low-noise and load-pull characteristics measured at W-band will be reported in the near future. These co-optimized epi/device structures and simple fabrication process ensure reliable and manufacturable GaN HEMT technology.

MULTI CHANNEL BRIDGE HEMT TECHNOLOGY

The second device technology is designed to increase transistor's drain current density, reduce R_{on}, and improve device-level linearity for wideband RF switch and linear PA applications. Fig. 2(a) illustrates a multi-2DEG-channel Buried Dual Gate (BRIDGE) HEMT. The epitaxial structure consists of 24 stacked 2DEG channels, with each channel being formed in an AlGaN/GaN/AlGaN quantum well (QW) HEMT. The n_s in each channel is controlled by a Si doping concentration in the AlGaN barrier layer. We optimized Si doping to ensure that every channel in the stacked structure has the same n_s of 2.25×10^{12} cm^{-2} and a net n_s of 5.4×10^{13} cm^{-2}, with high electron mobility of >1,500 cm^2/V·s. An electron confinement in the QWs improves electrostatic isolation between the source and drain under high drain bias. The source and drain ohmic contacts are formed by MBE regrowth of n+GaN on the multi-channel sidewalls. The parallel connections between the n+GaN and multiple 2DEG channels

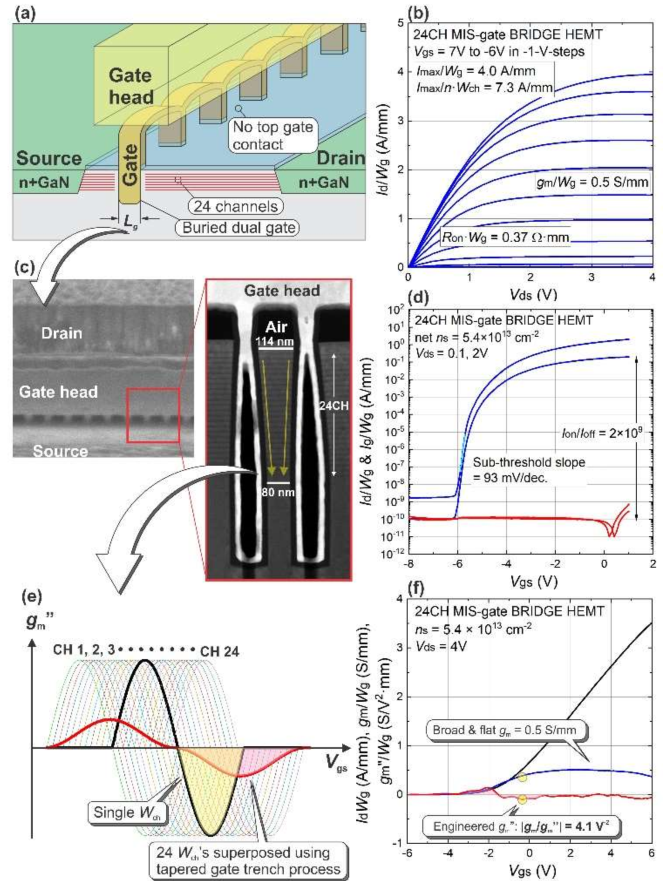

Fig. 2. Multi-channel buried dual gate (BRIDGE) HEMT technology (a). SEM of the BRIDGE gate and cross-sectional TEM images of the buried gate feet (c). Output (b), and transfer (d), (f) characteristics. Linearity enhancement through g_m'' (second derivative of g_m) superposition technique (f).

enabled an extremely small R_{ac} of 0.03 Ω·mm. The gate feet with or without a gate dielectric (Al_2O_3) are buried in narrow and deep trenches and laterally contact the 2DEG channels (Fig. 2(c)). A distance between the adjacent buried gate feet set a channel width (W_{ch}). The gate head that connects the gate feet is deliberately separated from the epitaxial surface. This enables; (1) only the lateral gate field controls the channel current, (2) a high electric field region is not formed on the top surface, suppressing the current collapse, and (3) parasitic gate capacitances associated with top gate contact are minimized. In essence, the BRIDGE HEMT operates like a MESFET by taking advantage of its linear performance while utilizing multiple 2DEG channels for high-current and low R_{on} operation. The low 2DEG density per channel (n_s = 2.25×10^{12} cm^{-2}) was chosen to (i) increase W_{ch} modulation efficiency by the lateral gates, and (ii) maximize an electron velocity under high electric fields [2].

Fig. 2(b), (d), and (f) show DC characteristics of the 24-channel BRIDGE HEMT with a 15-nm-thick Al_2O_3 gate dielectric. The device exhibits a record-high current density

of 4.0 A/mm with a low of R_{on} of 0.37 Ω·mm, a large I_{on}/I_{off} ratio of >10^9. The device has a built-in linearity enhancing feature. As shown in the cross-sectional TEM image (Fig. 2(c)), the device has slightly tapered gate trenches, and thereby the channel width of the stacked channels gradually decreases in the depth direction. An overall transfer curve of such a device is a result of superposing multiple transfer curves with slightly different threshold voltages. Fig. 2(e) compares mathematically calculated second derivative of g_m (g_m") curves for a device with a single channel width and a device with 24 channels with adjusted threshold voltages. The superposition technique reduces the g_m" peak height as well as its slope, which improves linearity performance and its sensitivity to any fluctuation of the applied voltage. The measured transfer characteristics exhibits a broad and flat g_m of 0.5 S/mm with greatly reduced g_m" due to the superposition. This leads to a greatly increased g_m/g_m" to 4.1, as compared to 0.6 of a single channel BRIDGE HEMT and 0.26 of our conventional T-gate HEMT. We are currently developing a wideband (DC to >70 GHz) RF switch MMICs based on the BRIDGE HEMT technology.

The 6-channel BRIDGE HEMTs with a Schottky gate developed for millimeter-wave PA applications are reported in ref. [3, 4].

Micro-Scale Device Cell Array Technology

With the increasing power density of transistors, the maximum RF output power obtained from a PA MMIC is eventually limited by self-heating. One approach to address this limitation is to combine the GaN HEMT epitaxial materials with a material that has high thermal conductivity, such as diamond, to reduce the thermal resistance (R_{th}) of the transistor [5]. Another way to reduce R_{th} of a transistor is by distributing the heat across the entire area of a PA cell. Figure 3(a) depicts our proposed concept of using an array of hexagonal micro device cells, aligned with the GaN crystal m-planes, to construct a PA cell. Unlike conventional PA cells that use a multi-gate-finger configuration, this micro-array structure enables to distribute heat over the entire area of the PA cell, which reduces the local heat flux. The source, drain, and gate electrodes are connected 3-metal level interconnect.

Fig. 3(b) and 3(c) show thermal simulation results obtained for a conventional PA cell with two gate fingers, whose gate-to-gate pitch is 100 µm, and a micro-arrayed PA cell. The PA cell size targeted for Ka-band frequencies is 80 µm × 200 µm. The 2-finger cell has a total gate periphery of 160 µm, while the micro-arrayed cell has a total gate periphery of 200 µm. The dissipated power density is 20 W/mm, which correspond to an area density of 200 W/mm^2 and 250 W/mm^2 for the 2-finger cell and micro-arrayed cell, respectively. In the thermal simulation, we assumed: (i) thermal boundary resistance (TBR) of the AlN nucleation layer is 10 m^2·K/GW, (ii) the thickness and thermal conductivity of the SiC substrate is 50 µm and 350 W/m·K, (iii) the thickness and thermal conductivity of the AuSn eutectic material is 20 µm and 57 W/m·K, and (iv) a 500-µm-thick Cu heat sink with a thermal conductivity of 180 W/m·K, and (v) a fixed temperature of 50°C at the back of the Cu heat sink. The simulated peak temperature rise for the 2-finger cell is 250°C, while that for the micro-arrayed cell is only 90°C. This result indicates effectiveness of micro-array concept to reduce the transistor R_{th}. Fig. 3(d) shows pulsed and static I-V characteristics of a micro-arrayed PA cell that has a total gate periphery of 621 µm within a 100 µm × 40 µm area. The thickness of the SiC substrate is 500 µm without a heat sink. The device exhibits a static current of 0.7A at a V_{ds} of 15V,

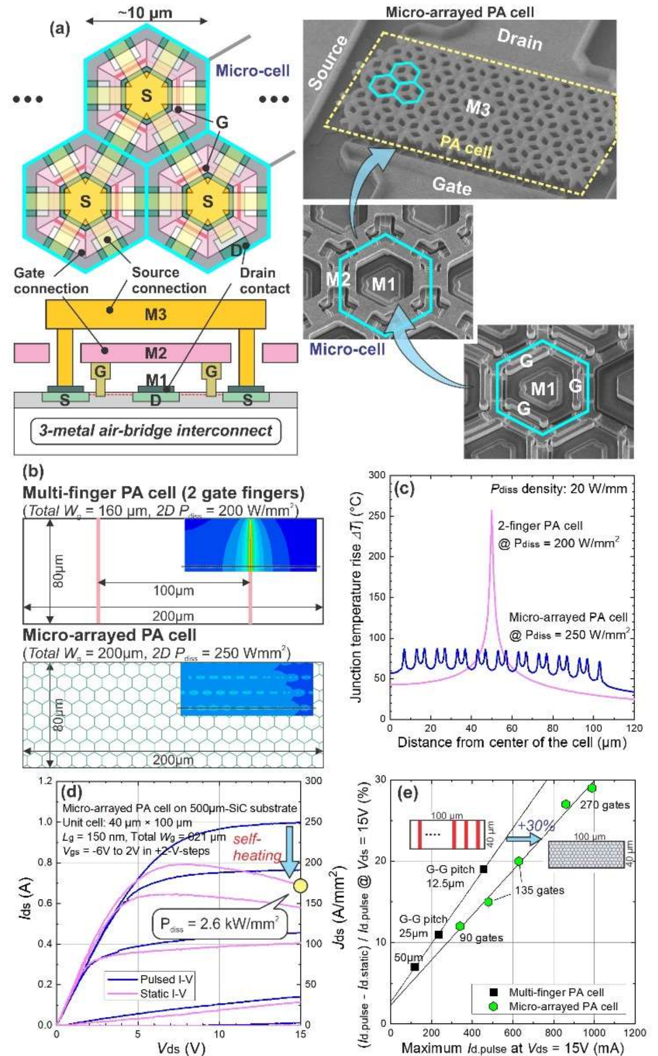

Fig. 3. Micro-scale device cell array to reduce transistor's thermal resistance by uniformly distributing heat across the entire area of a PA cell (a). The source, drain and gate electrodes are connected using 3-metal level interconnect. Thermal simulation results performed for a conventional multi-finger PA cell and micro-arrayed PA cell (b), (c). Pulsed and static I-V characteristics of a fabricated micro-arrayed PA cell, showing a current drop at increased DC power dissipation densities (d). Comparison of the current drop between multi-finger and micro-array PA cells (e).

which corresponds to an area power dissipation density of 2.6 kW/mm^2. The amount of the current drop relates to the junction temperature rise due to self-heating. Fig. 3(e) compares the current drop as a function of the dissipated power density between the multi-finger and micro-array devices, demonstrating a reduced self-heating in the micro-array devices due to effective heat distribution. This technology combined with a high thermal conductivity diamond heat spreader will drastically improve thermal properties of GaN HEMTs, and thereby increase transistor's output power density, efficiency while improving device reliability.

CONCLUSIONS

In this paper, we discussed three key innovations to address the performance trade-off in the present millimeter-wave GaN HEMTs: (i) co-optimized epitaxial/device structures for low-noise and PA applications at W-band frequencies, (ii) multi-2DEG-channel BRIDGE HEMT technology for wideband RF switch and linear PA applications, and (iii) micro-scale device array concept to reduce transistor thermal resistance at the device level for reliable device operations.

ACKNOWLEDGEMENTS

The authors would like to thank our colleagues in Fabrication Operations Group for their dedicated work with wafer processing.

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