Scaled β-Ga_2O_3 MOSFETs with Pulsed Laser Deposition-Regrown Ohmics

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Abstract

We demonstrate a method for facile, high-yield regrowth and liftoff of highly doped β-Ga_2O_3 deposited by pulsed-laser deposition and lifted off using a bilayer liftoff mask. This technique provides major advantages in yield and ease-of-use compared to previous liftoff approaches. The technique is then used to fabricate highly scaled MOSFETs with regrown ohmics with on-resistance as low as 21.7 Ω·mm for a 1 µm channel device at $V_{gs} = 0$ V. Reducing parasitic resistance is critical to advancing the performance of such highly scaled devices wherein parasitic resistance makes up a significant percentage of device on resistance.

INTRODUCTION

Beta-phase gallium oxide (β-Ga_2O_3) is an emerging ultra-wide band gap (UWBG) semiconductor with potential applications in power electronics, solar-blind optoelectronics, and radio-frequency applications [1]. Its superior performance is due to its large band gap of 4.8 eV and commensurately high critical electric field strength estimated at 8 MV/cm [2].

Eliminating parasitic resistance is critical for real-world devices to approach the theoretical maximum performance of β-Ga_2O_3 [3]. This is especially critical in β-Ga_2O_3 due to its relatively high bulk resistivity compared to SiC or GaN: Devices with inefficient scaling, process misalignment, or excess source-gate (access region) spacing suffer from reduced on-resistance R_{on} with no added benefit to breakdown voltage $V_{bk.}$ Contact resistance R_c is a significant contributor to R_{on}, especially as device channel lengths are scaled down and sources of parasitic resistance constitute a significant portion of device resistance. Management of R_c through selective-area doping is paramount to achieving low R_{on}, but current approaches have practical limitations. Ion implantation doping has not been demonstrated to achieve carrier concentrations as high as in situ doping has [4], and requires high-temperature activation anneals that can diffuse dopants and impurities[5]. Selective-area regrowth and liftoff can achieve much higher doping levels [6] but may be difficult due to the high chemical resistance of β-Ga_2O_3, often requiring long processing times

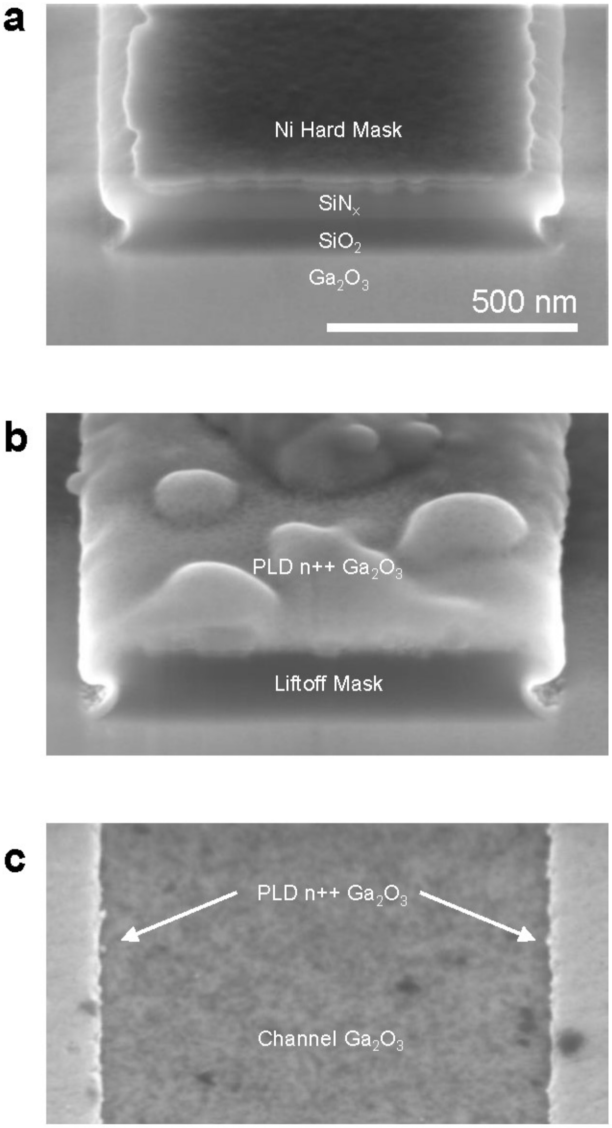

Figure 1 a) SEM-FIB cross-section of a T-shaped bilayer liftoff mask consisting of 100 nm SiN_x and 100 nm SiO_2, defined by RIE etch with nickel hard mask; b) the same liftoff mask with 50 nm OF PLD Ga_2O_3, showing conformal regrowth; c) the same region after 30 minutes of sonication in BOE to remove the liftoff mask and reveal the underlying Ga_2O_3.

and yielding unpredictable results. Here, we report a method for the regrowth and liftoff of highly conductive $\beta\text{-Ga}_2\text{O}_3$ films grown by pulsed laser deposition (PLD), which greatly reduce R_c, and thus R_{on}, of highly scaled $\beta\text{-Ga}_2\text{O}_3$ transistors.

METHODS

A 100 nm Si-doped $\beta\text{-Ga}_2\text{O}_3$ channel layer was grown homoepitaxially on an Fe-doped (010) substrate by molecular beam epitaxy. Hall measurements showed a carrier concentration of 8.03×10^{17} cm^{-3} and a mobility of 71.4 cm^2/Vs. A bi-layer mask consisting of 100 nm SiO_2 and 100 nm Si_3N_4 was deposited by plasma-enhanced chemical vapor deposition (Figure 1). Regions for regrowth were defined via Ni hard mask and reactive ion etching, followed by a controlled wet etch in dilute buffered oxide etch (BOE) to undercut the SiO_2 layer. Si-doped $\beta\text{-Ga}_2\text{O}_3$ was regrown via PLD at a nominal thickness of 50 nm, and liftoff was performed by sonicating in BOE for 30 minutes, followed by a DI rinse. Micro-van der Pauw Hall measurements showed the regrown layer to have a doping averaging 1.9×10^{20} cm^{-3} and an average mobility of 36 cm^2/Vs. Fabrication of MESFETs and MOSFETs with channel lengths of 1 and 2 µm was completed using a 23 nm Al_2O_3 gate/passivation oxide, annealed Ti/Al/Ni/Au ohmic contacts, and Ni/Au T-gates with a stem gate length of 200 nm (Figure 2).

Devices showed high yield with good contact quality. Extrapolating R_c from excess resistance versus channel length [7] across all well-behaved devices estimated a R_c of 1.7±2.6 Ω·mm with 1 µm devices averaging an R_{on} of 26 ± 3 Ω·mm and 2 um devices averaging an R_{on} of 44 ± 6 Ω·mm. The best-performing device under test (DUT) was a 1 µm channel-length MOSFET with an R_{on} of 21.7 Ω·mm, transconductance of 25.9 mS/mm, maximum current I_{max} of 172 mA/mm at $V_{\text{ds}} = 8$ V, $V_{\text{off}} = -11.2$ V, and an on-off ratio $I_{\text{on}}/I_{\text{off}} \sim 10^7$ (Figure 1 a and b). Catastrophic breakdown of similar 1 µm channel MOSFETs occurred at > 114V (Fig. 1 c), at an estimated peak field of 2.75 MV/cm. This corresponds to a Power Figure of Merit (PFOM) of 59.9 MW/cm^2 and an estimated Huang's Material Figure of Merit (power-switching figure of merit, HMFOM) of 8.8 (W/C)$^{1/2}$ (Fig. 1 d).

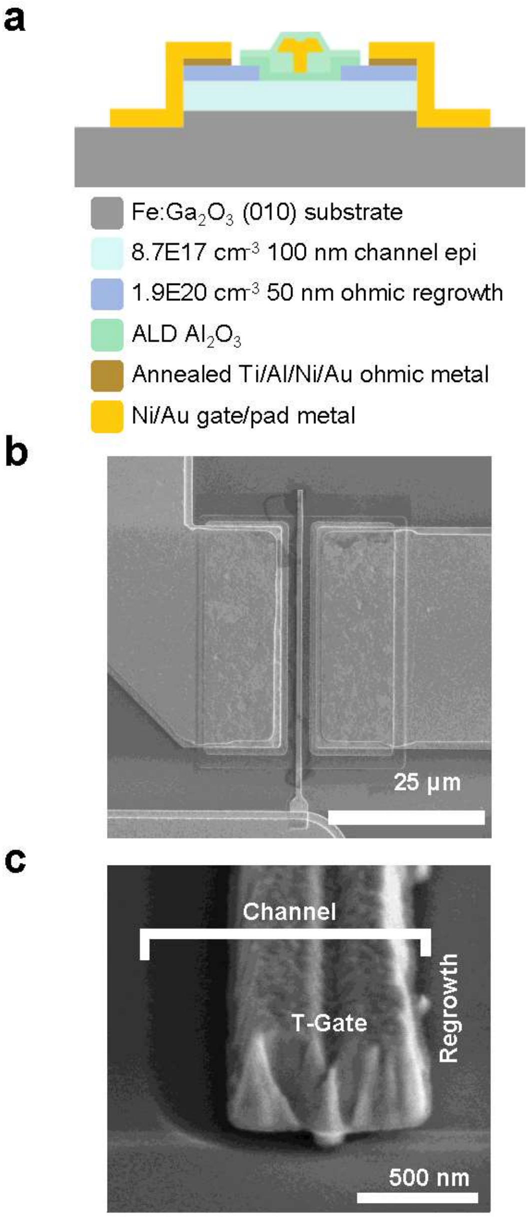

Figure 2 a) Schematic of a MOSFET (the DUT) b) plan view SEM micrograph of a 1 µm channel MOSFET; c) side view of a 1 µm channel MOSFET showing the regrown ohmics, channel region, and T-Gate.

DISCUSSION

Increasing process reliability, ease, and yield is critical to the successful commercialization of a new semiconductor technology. This is especially true in $\beta\text{-Ga}_2\text{O}_3$ where the cost basis is likely to be a major driver of adoption [8]. The bi-layer liftoff mask presented here increases the yield of ohmic regrowth significantly while also greatly reducing processing time. This process yields not only high-quality hero devices such as the DUT, but also increases device yield and uniformity across the sample compared to previous liftoff methods Larger devices [9] see smaller improvements in device R_{on} (and subsequently in related figures of merit) from reducing parasitic resistances such as R_c, as the intrinsic resistance of the large device channel dominates R_{on} at large drift lengths. Excellent device performance has previously been demonstrated in the regime of device operation requiring V_{bk} in the hundreds or thousands of volts [9], [10]. $\beta\text{-Ga}_2\text{O}_3$ offers potential performance benefits for devices with $V_{\text{bk}} <$ 100 V as well, such as smaller smaller footprints, lower costm and lower R_{on} for a given V_{bk} versus other materials systems. Successful fabrication of such devices requires the minimization of parasitic resistances that dominate device R_{on} for highly scaled devices, as well as reliable control over

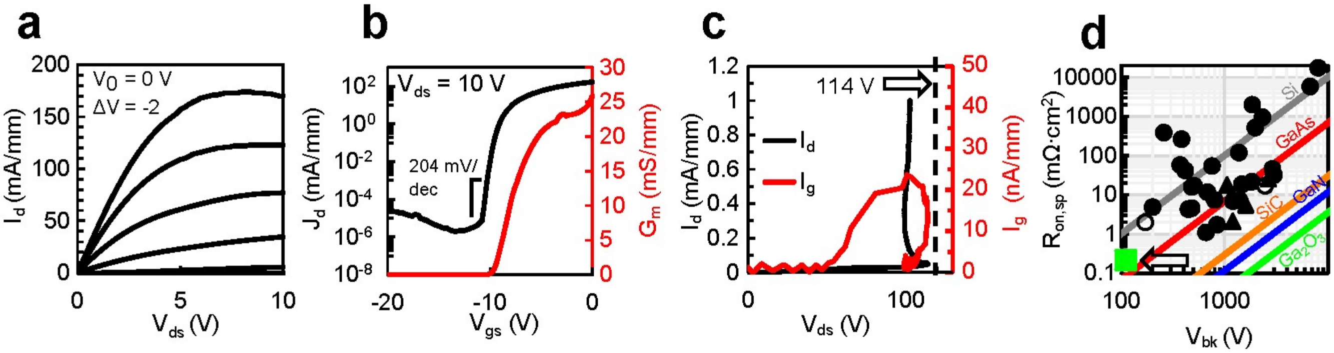

Figure 3 a) Transfer characteristics and b) family of curves of the DUT; c) breakdown performance of a similar 1 μm channel MOSFET; and d) PFOM plot of other Ga_2O_3 transistors, including MESFETs (open circles), MOSFETs (closed circles), and FINFETs (triangles) with the DUT in green.

device dimensions even at the submicron scale. The liftoff method presented here provides both, as evidenced by the high yield of highly scaled devices appropriate for sub-hundred-volt device operation.

CONCLUSION

Highly scaled β-Ga_2O_3 transistors were fabricated using a novel regrowth and liftoff method that showed increased yield and ease of manufacture compared to previous methods. The resultant devices had low R_c and low R_{on}, resulting in improved device performance in the <100 V regime. These results demonstrate the feasibility of manufacturing β-Ga_2O_3 devices in a voltage regime not previously demonstrated in β-Ga_2O_3, while achieving a BFOM in excess of the unipolar Si limit and competitive with previous β-Ga_2O_3 devices.

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