Improving the yield for GaN-on-Si HEMT devices for power applications

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Abstract

GaN-on-Si devices for power conversion are on the way to volume production, replacing conventional Si devices. We address the need for improved yield by improved hardware of our batch reactor. We observe that improvement of the AlGaN barrier uniformity is directly reflected in the threshold voltage (V_{th}) range, giving a within wafer range of 0.2 V for an E-mode device. To extent the voltage range beyond 650 V, we scale up the buffer thickness > 7 µm and achieve a breakdown voltage > 1200V.

INTRODUCTION

GaN-on-Si High HEMTs are becoming the most important building block for highly efficient power conversion. Due to the unique material properties and switching speed of GaN, power converters can be operated at significant higher frequency, allowing to reduce passive components in terms of size and weight.
As GaN power devices are in transition into volume production, focus is shifting from performance to yield and cost.
The method of choice for mass production of such GaN HEMT device stacks is MOCVD, particularly on large-diameter (>150 mm) Si (111) wafers due to their low cost, availability, and compatibility with existing Si fabs. Here we are showing how optimized MOCVD hardware and process can significantly contribute to increased yield and therefore reduced cost.

EXPERIMENTAL

A typical device stack for an E-mode device is shown in Figure 1. It consists of an AlN nucleation, an AlGaN super-lattice (SL) and GaN:C buffer, which thicknesses are typically scaled to the desired vertical breakdown voltage, V_{br}. The active device is formed by the GaN channel, AlGaN barrier and p-GaN gate. The AlGaN barrier and p-GaN properties are adjusted in a way that the 2DEG is fully depleted. V_{th} and V_{br} are the key parameters with their inhomogeneities limiting the on-wafer yield of such a stack. V_{th} is influenced by the AlGaN barrier alloy composition, AlGaN barrier thickness, active Mg doping level in the p-GaN, and C levels in all GaN channel, AlGaN barrier and p-GaN, rendering the homogeneity of V_{th} a difficult art to master [1]. The breakdown voltage is mainly influenced by the buffer thickness, alloy composition of the SL and carbon level of GaN:C and SL.

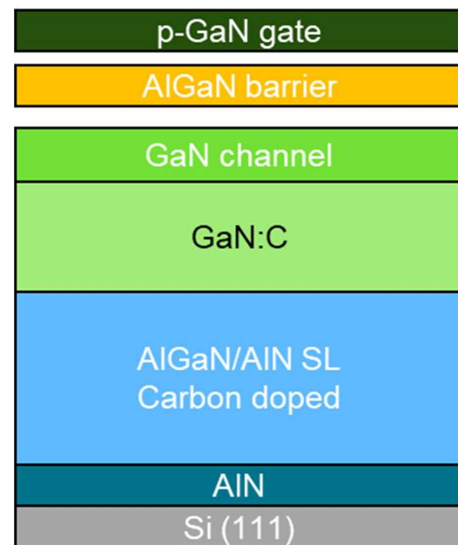


Figure 1 Typical E-mode stack GaN-on-Si with a total stack thickness of ~4.5 µm

To obtain uniform AlGaN growth, we optimized the hardware of our production-proven platform, the AIXTRON G5+ C Planetary® MOCVD batch reactor resulting in our next generation platform for 8x150 mm and 5x200 mm configuration. Particularly, the satellite (wafer holder) was optimized to ensure a uniform temperature distribution and at the same time omitting any interaction of neighboring graphite or SiC parts.
To demonstrate the capability of our next generation platform, a device stack as schematically shown in Figure 1 is deposited on 200 mm Si (111). Growth is initiated by an AlN nucleation, followed by an AlGaN/AlN SL buffer with a thickness of ~3 µm. Subsequently, a GaN:C layer of 1 µm is deposited acting as a back-barrier for the GaN channel.

The carbon doping of the buffer layers is employed by using an extrinsic carbon source [2,3]. By this, a uniform and easy to control carbon level is achieved. A 200 nm unintentionally doped (uid) GaN channel is followed by a thin AlGaN barrier, which is capped with a p-GaN gate.
Full device processing was performed at the imec pilotline, Leuven, Belgium using the 650 V GaN-on-Si process to access device parameters like V_{br} and V_{th}.
In a second variation, five different samples for which the buffer thickness was gradually scaled up to more than 7 µm have been grown. The increase in buffer thickness was mainly achieved by increasing the SL part of the buffer. For this second set of samples, V_{br} was assessed.

RESULTS

First, the results for the first set of samples are described. The vertical breakdown voltage at room temperature with a current criterion of 1 µA/mm² is given in Table 1. With a total stack thickness of ~4.5 µm, an excellent average breakdown voltage of 906 V is achieved. The narrow V_{br} on-wafer distribution is validating the advantage of carbon doping with a dedicated source as well as the uniformity in our next generation platform.

TABLE I

Average V_{br} (V)	905.8
1σ (V)	19.9
1σ (%)	2.2%
Absolute Range (V)	65
Relative Range (%)	7.2%

Vertical breakdown at room temperature @ 1 µA/mm²

The Al composition of the AlGaN barrier was assessed by room temperature PL on a stack as sketched in Fig. 1 but without p-GaN cap. A typical Al distribution across a 200 mm wafer is shown in Figure 2. As figure of merit, the area within a certain specification is used. For an allowed 1% Al range up to 99.5% are achieved. In Table 2, an overview of a full run is given, showing almost no difference between all individual five wafers.

TABLE II

Wafer	Average Alloy composition (%)	Area in spec (%)
1	22.6	99.5
2	22.6	98.4
3	22.7	98.4
4	22.6	98.2
5	22.6	99.1

Average Al composition and area in spec for a 1% Al bin of a full load run, 2 mm edge exclusion

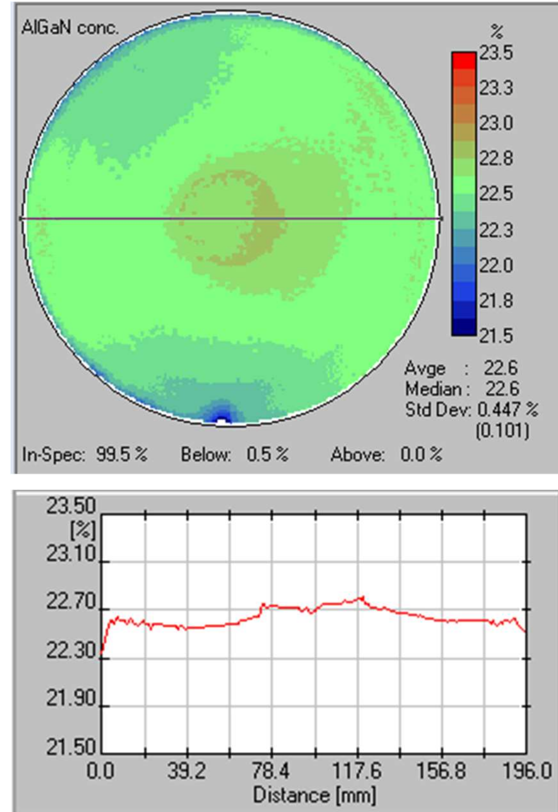


Figure 2 Al composition mapping by PL of a 200 mm wafer showing a very uniform Al distribution across the wafer. 2 mm edge exclusion was applied.

The AlGaN barrier thickness was assessed using X-ray reflectivity (XRR) also on a stack without pGaN cap. A relative thickness variation of below 4% across the 200 mm wafer is extracted (not shown). A wafer map of the V_{th} (E-mode stack, Fig. 1) is given in Figure 3. The V_{th} extracted at maximum transconductance is 2.2 V with a range of only 0.2 V reflecting the uniform AlGaN barrier properties.

For the second set of experiments, the impact of buffer thickness on V_{br} is given in Figure 4. Although the stacks for the individual data points have been individually optimized, an almost linear dependency of V_{br} with the total stack thickness is observed.
An IV curve for wafer center and edge of the 7.3 µm-thick sample is also given in Fig. 4, showing a $V_{br} > 1200$ V can be achieved by GaN-on-Si on our high-volume production system.
It is worth mentioning that for buffer thicknesses above 5 µm, we see the need to use substrates with a non-standard thickness of 1 mm. For a total stack thickness above 7 µm, substrates with a thickness of 1.15 mm are the preferred choice. By using an adjusted substrate thickness, post-epi bow can be well maintained below 50 µm.

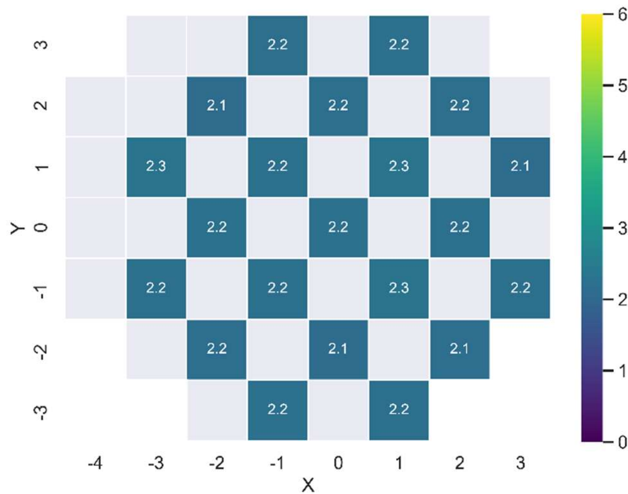
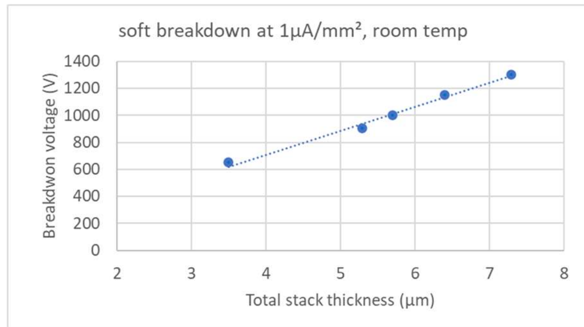


Figure 3 V_{th} map of a 200 mm wafer



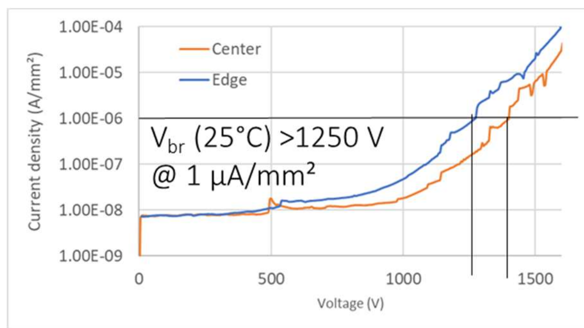


Figure 4 top: breakdown voltage as function of buffer thickness, bottom: IV curves of the 7.3 µm sample

Conclusion

Excellent on-wafer yield for V_{th} and V_{br} have been shown on our next gen GaN platform in a 5x200 mm configuration. We attribute the tight V_{th} distribution to the optimized hardware, resulting in a narrow Al distribution in the AlGaN barrier within wafer and wafer-to-wafer. Further, we have shown how breakdown voltage for GaN-on-Si can be scaled beyond 1200 V by increasing the stack thickness above 7 µm, extending the voltage range for future GaN devices.

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Acronyms

MOCVD: Metal organic vapor deposition
HEMT: High electron mobility transistors
E-mode: enhancement mode
Vbr: vertical breakdown voltage
SL: super lattice
Vth: threshold voltage
PL: photoluminescence
XRR: x-ray reflectivity
IV: current voltage