Perspective of power module packaging technology

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Abstract

This paper describes the assembly and interconnection technologies, design and trends of high-power semiconductor modules. The electrical performance of the modules is determined by matching module design and chip characteristics. To achieve a high reliability, a semiconductor metallization is necessary that is tailored to the respective connection technology [1]. Optimized solutions, such as .XT^{TM} technology, are presented and discussed in terms of design, material, process and reliability.

INTRODUCTION

Frame-based multichip power semiconductor modules are developed for currents of 15 A up to several kA at voltages of 600 V to 6.5 kV. IGBTs are used as switches in a wide variety of configurations. Depending on the output current, however, products can consist of a multiphase topology or only a single switch.

Economically, IGBT dies can only be manufactured up to a size of about 250 mm². For large currents, up to 30 dies are therefore connected in parallel in one package.

The technologies and design features used to create such packages are described below.

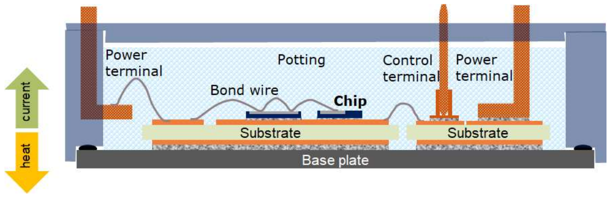

Fig. 1. Schematic cross-section of a power semiconductor module

STRUCTURE OF POWER SEMICONDUCTOR MODULES

The basic structure of a multichip frame-based power module is shown in Figure 1. In addition to the chips, a central functional element is the ceramic circuit carrier, referred to below as the substrate. It is clad with copper or aluminum on both sides. The front side contains a structured layout to separate different electrical potentials, and dies are mounted on top of the structure. The front-side contact of the chips is usually made using wedge-wedge aluminum wire bonds.

Ceramic substrates can be safely processed in modules up to a size of approx. 50x60 mm². Very large currents or sophisticated electrical topologies such as the 3-level topology cannot be implemented on a single substrate. Therefore, several substrates are often mounted on a base plate made of copper or AlSiC.

Modules also contain contacts for power and control connections. To ensure insulation, the entire interior of the module is filled with silicone gel. This is shown in Figure 2 in the example of a 1500 A module with a nominal voltage of 3.3 kV for traction applications.

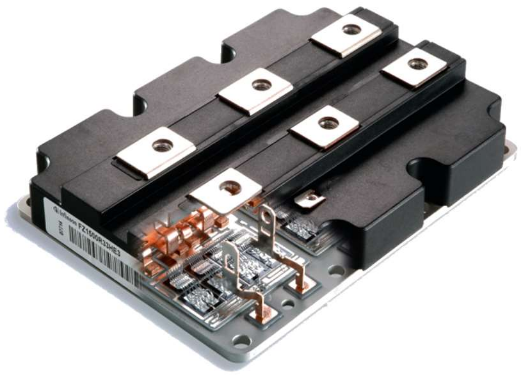

Fig. 2 traction module 3.3 kV, Inom 1.5 kA

The operation of power semiconductors is always subject to losses, e.g. conduction and switching losses. Total loss densities of about 100 W/cm² and a maximum junction temperature of 150 to 200°C are common. Depending on the application, these temperatures occur repeatedly, or in the event of an overload. All insulation materials and connection technologies must be designed to respect these boundaries.

MATERIALS AND PROCESSES

Frame-based power modules are built from substrates with a ceramic insulator. The ceramic material allows insulation voltages of up to 10kV to achieve and provides a good heat dissipation from the chips to the cooler. Suitable materials for the substrate include Al_2O_3, AlN and Si_3N_4 although there is no optimum substrate for all applications. Several parameters have to be considered for the selection. Unfortunately, the material AlN with the best thermal performance has the lowest mechanical strength. And Al_2O_3 with the lowest thermal conductivity is the cheapest.

Design parameter include the thickness of the ceramic and metal lamination, which can be used to control the thermal performance via heat spreading. A 0.32 mm thick Al_2O_3 substrate shows similar thermal performance as a 0.63 mm thick Si_3N_4 substrate at a quarter of the price, but with reduced mechanical stability. Therefore, substrates made of Al_2O_3 as opposed to Si3N4 will be chosen for cost-sensitive applications, while Si_3N_4 will occasionally be used in automotive applications for safety reasons. The reduced mechanical strength can be compensated by an optimized frame design.

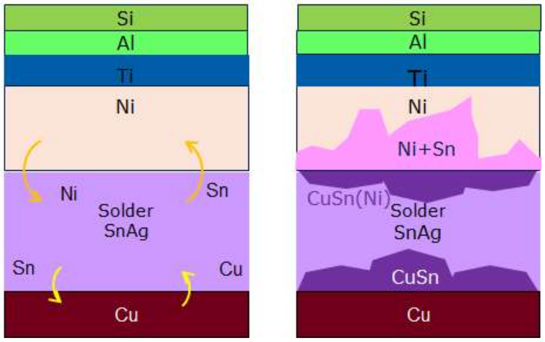

Fig. 3. Schematic representation of a backside metal stack before and after the soldering step

Dies are usually attached to the substrates with a tin-based solder. For this purpose, the back side is provided with a metal stack, which is sketched in Figure 3. During soldering, a diffusion processes takes place between the Ni layer and the solder [2]. In this process, Ni is ablated. The metallization must be designed to create a stable diffusion layer without Ni being fully consumed.

NEW JOINING TECHNIQUES

The lifetime of a chip connection is mainly limited by active power cycles. The solder is sandwiched between chip and substrate, and can expand only in the Z-direction during active heating. This leads to fatigue of the solder body [3].

To extend the power cycling capability, silver sintering has been introduced. In general, sintering is the transformation of a loose metal powder into a firmly bonded porous structure. In this context Ag sintering is a pure solid-state diffusion without melting. The interconnect is formed by sintering smallest sphere-like Ag particles, activated at low temperature (<300°C) and pressure [4]. This die interconnect technology is performed on noble metal surfaces for the sintering materials Ag and Au. However, it is meanwhile possible to sinter on Cu. Compared to solderable chip metallization, sinterable connections are thinner, since alloys do not have to be considered.

Figure 4 compares the reliability of a soldered 4th generation IGBT (IGBT 4) as a reference with a sintered connection. The sintered one is about 20 times more reliable compared to a high-quality solder connection [5], [6].

While tin-based solder joints will fatigue at junction temperatures above 150°C, a sintered joint can be used up to temperatures exceeding 200°C. Depending on the application, a higher power cycling capability can therefore be achieved with the sintered connection at the same junction temperature. Or a module can be operated at a higher junction temperature with a reliability comparable to tin-based solders. This leads to an increased output power.

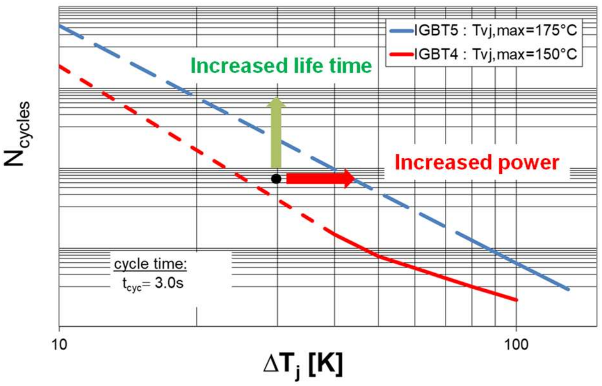

Fig. 4. Comparison of the power cycling reliability of a Sn based solder joint and Al bond wires (red curve) as reference with silver sintered joint and Cu bond wires as advanced technologies (blue curve).

The front-side of high-power chips is connected using thick wedge-wedge Al or Cu bond wires, which usually have a diameter of 300 to 500 µm. Due to the higher electrical resistance of Al, these wires heat up much more than Cu ones. However, the effect depends on the loop length. A bond wire length of less than 8 mm is difficult to optain. With Al therefore, a current-carrying capacity of about 25 A per 400 µm bond wire is realistic. With Cu, the current can be doubled. In 2015, Infineon introduced the combination of Cu bonding technology and silver sintering under the name .XT™ . This is the most reliable joining technology for multichip power modules available on the market [7].

The combination of sintering and Cu wire bonding is well balanced in terms of reliability. In a combination of using Al bond wires and a sintered back side, the wire connection would fail much earlier, and the potential of the sinter connection would not be exploited. Nevertheless, this combination with a 15 to 20 µm thick Ag sinter layer is used in some applications to improve the thermal path compared to an 80 to 100 µm thick solder.

For a reliable connection, the Cu bond technology requires a pure Cu front side on the chip. The application of a Cu layer on an Al spacer leads to accelerated fatigue of the Al layer

[8]. Recently, another wire bonding material has become available that consists of a Cu core and an Al skin. This allows a combination of copper bonding wire and a favorable Al metallization [9]. Owing to its mechanical and electrical parameters, Cu is superior to Al for bond interconnects.

Compared to an Al wedge on an Al chip-frontside CuCorAl (Cu core with Al shell) improves the power-cycling lifetime by a factor of 3 to 5. With Cu on Cu the power-cycling lifetime improvement of > 10 can be achieved.

MODULE DESIGN

Using the technologies described, power semiconductor modules can be designed for specific applications. Figure 5 compares two basic load profiles for general purpose drives (GPD) and servo applications, each with two working modes. The GPD profile on the left is characterized by long, uniform loads that heat up the entire module. The load on the chip-related joining technology (bonding wires, solder) will be low. For this profile, good heat dissipation, e.g. using an AlN substrate, is very helpful, but may be too expensive. Alternatively, thin Al_2O_3 ceramics can be used. In this case, however, the mechanical stability of the module must be ensured by a sophisticated frame design.

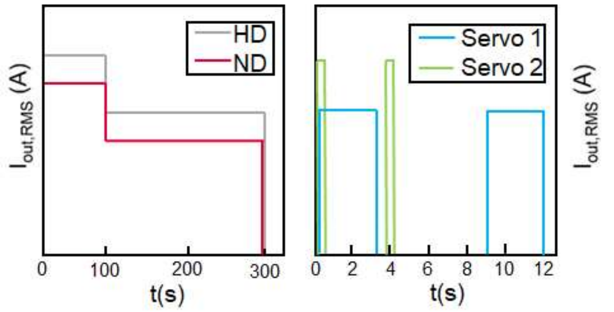

Fig. 5. Schematic load profiles for general purpose drive applications (ND: normal duty; HD heavy duty) on the left and servo applications on the right.

The profile of a typical servo application is shown on the right of Figure 5. One can see very short current loads. The heat generated in the switch only warms the local areas around the chip. Since substrate and base plate remain practically cold, large thermomechanical stress occurs in the chip connections. In the case of servo applications, as illustrated on the right, the time constants are so small that a high thermal conductivity of the substrate has little influence on the lifetime. In this case, however, a larger chip leads to improved heat spreading, and therefore, lower temperature and stress resulting in increased lifetime.

Alternatively, with the potential of a sintered layer and Cu bond wires, sufficient or increased reliability can be achieved despite a small chip. However, two points must be considered. First, the effect depends on the position of the junction in the semiconductor. In the case of MOSFETs, it is located near the chip frontside. For pulsed loads, a thick Cu layer on the front side is more effective than an optimized backside connection [10]. In modern IGBTs like trench IGBTs, however, the junction is located close to the back side. Here, a very thin and highly heat-conductive backside connection is more effective. On the other hand, the choice of components depends on the area available in the package. In small packages, there is often not enough space to integrate more silicon. On the other hand, the additional costs of silicon must be weighed against the additional costs required for an improved joining technology.

Power semiconductor modules are used in a large number of applications, each with specific load profiles and lifetime requirements. Formerly, one module design with one chip variant covered many customer requirements. Today, modules are optimized to fit the requirements of the dedicated application. These products run in relatively small quantities and require very flexible packages. Particularly suitable for this are packages like Infineon's EasyPACK^{TM} family, which are designed as a modular system. They enable to freely position the connection pins in the lateral area, a feature that offers a high degree of flexibility for layouts.

PACKAGING WIDE BAND GAP SEMICONDUCTORS

For an optimal use of wide band gab semiconductors, the package design should be adapted. In classical applications like GPD, IGBTs are usually operated at switching frequencies of 400 Hz to 16 kHz and a dV/dt of less than 5 kV/µsec. With the new SiC devices, it is possible to increase the switching frequencies and slew rates significantly.

To prevent overshoot-induced derating at turn-on and turn-off, the DC-link path should be designed with low stray inductance [11]. For clean switching with reduced overshoot, gate-source coupling should be optimized. In both cases multilayer structures on substrates would be helpful. An example is the structure presented by ABB in an approach called LinPak [12].

Electro-mobility is another young application in the field of high-power modules. It stimulates multiple innovations. On the one hand they are driven by the requirement of loss reduction directly leading to an increased range. On the other hand, modules for electro-mobility are going to be manufactured in much higher quantities than in the industrial sector. The economy of scale therefore enables solutions that would not be financially viable in the industrial sector with its smaller quantities per package variant.

In the automotive sector, DC-link voltages are limited to about 1000 V resulting in low insulation requirements compared to industrial applications. Thus, solutions, such as the eMPack® demonstrator from Semikron, have been developed to meet these requirements [13]. In this design, using a flexible PCB, the DC-link potential is routed as a strip line to the center of the module. Similar to a clip, the flexible PCB is sintered to the chips and to the substrate at specific locations. These are technologies that cannot be implemented in industrial modules with DC-link voltages higher than 1200 V. However, the design comes with a benchmark total inductance of 2.5 nH.

CHALLENGES AND OUTLOOK

With increasing junction temperatures, the use of Cu-based sintering pastes and diffusion-brazed joints may increase, since these joints are not weakened by higher temperatures. SiC components can be operated effectively at temperatures of around 200°C.

While chip joining technologies~~y~~ are available for these temperatures, mold compounds do not fulfill this requirement. Due to resistive self-heating, maximum temperatures of more than 230°C can be expected in the bond loop, even with Cu bonds. Today, no polymers are available that allow safe operation for the required lifetime of 5 to 30 years at the above-mentioned temperature.

In the future silicone compounds will be needed for such high temperatures. However, due to the huge quantities of identical modules in the automotive sector, epoxy resin mold compounds are permitted too. Hence, the development of suitable high-temperature polymers is to be expected in the future.

Newer the less inn all applications cost pressure limits the use of advanced technologies. This limits the trend to raise the junction temperatures. Therefore, a substantial number of new packages will still be based on Al bond wires and solder joints.

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ACRONYMS

GPD: general purpose drive