Expectations and Challenges of GaN Power Devices from an Application Viewpoint

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Abstract

In this presentation, expectations for GaN power devices, future applications, and market size will be described from the perspective of applications. In addition, realistic problems in realizing those applications such as low Vth, reliability issues, current collapse, lack of unified basic specifications across vendors, non-standardized packages (PKG), issues in mounting PCB design, etc. is also provided. Expectations and requests for device/process/implementation people will be discussed.

INTRODUCTION

Toshiba is one of the largest companies in the power device and system field with a long history. With regard to SDGs in recent years on a global scale, power devices have great expectations and responsibilities. There is a strong demand for higher efficiency, smaller size, and lower cost. Silicon power devices is nearing its limit dictated by the material properties.

Under such circumstances, there are high expectations for wideband semiconductors such as SiC and GaN. In fact, SiC has started to be applied to automobiles, railways, high-end inverters/converters, and we are entering the period of full-scale mass production. The market size of GaN power device is predicted to be one order of magnitude greater within a decade [1], although still the size is likely to be less than 1/3 of that of SiC [2] in 2027. Despite better Figure-of-Merit as Baliga summarized in [3] and high expectation to realize better power density by GaN power device, the market growth is slower compared to SiC. There still remains questions for the majority of power electronics engineers of how to apply GaN power semiconductors to one's specific application. GaN power devices, at this moment, is so different that it is more than just replacing Si with GaN in their power circuitry. This is a significant barrier which prevents the insertion of GaN power devices. This paper describes expectations as well as challenges of GaN power devices starting from application viewpoints.

EXPECTATIONS FROM APPLICATION VIEWPOINTS

Superior physical properties of GaN, such as wide bandgap, high mobility, high critical field and high saturation velocity in comparison to Si, provide better power conversion efficiency. In addition, thanks to the highest mobility and saturation velocity among three, GaN power device can switch in the highest frequency, more than one order of magnitude higher than Si. This will generally result in smaller passive components, particularly inductor and transformer, which enables smaller equipment size. Non-existence of anti-parallel body-diode, which leads to almost zero reverse recovery losses, is another advantage of GaN devices. For this feature, low switching loss is sustained even at high frequency. For the reasons mentioned above, it is expected to realize power conversion equipment with both high-efficiency and high-power density by using GaN power devices, which distinguishes GaN from Si technologies. This is important motivation to introduce GaN power devices for applications such as AC adaptors, micro-inverters, server power supplies, and 5G/6G base stations. In these applications, not only does power conversion efficiency matter but also equipment size.

CHALLENGES FROM APPLICATION VIEWPOINTS

Motivation to use GaN power devices instead of Si and/or SiC is to achieve better power conversion efficiency and high-power density simultaneously with affordable cost. Realization of high frequency switching at mega-hertz frequencies without affecting system-level power conversion efficiency is essential as well as suppressing noise to comply with electromagnetic interference noise code. Emission noise could be one of the most serious issues as switching frequencies are close to regulated frequencies. Moreover, noise suppression is important to avoid erroneous turn-on of GaN power devices which result in ground fault of power electronics equipment.

To realize ideal efficiency and low noise under high frequency switching, parasitic inductances and capacitances must be minimized to avoid oscillation of the switching waveform. Therefore, PCB layout design is critical, especially between gate and gate driver loops as well as source and the ground loops. Generally, gate driver and GaN power semiconductors should be placed as close as possible each other to minimize parasitic inductances.

Reduction of parasitic inductances between device terminals of a discrete GaN power device is also important. Package type and assembly technology must be carefully considered to minimize parasitics. Moreover, integrating GaN power semiconductor devices and gate driver into one package could be a solution since the loops mentioned above

could be significantly reduced compared to those implemented on PCB.

Considering challenges from application viewpoints, the following three criteria are more emphasized during power semiconductor selection.

Criteria-1: Low on-resistance and parasitic capacitance to achieve good switching characteristics for low energy loss and low noise.
Criteria-2: Threshold voltage, Vth, more than ~2.5V, immune to noise, to avoid ground fault and to achieve fail-safe operation.
Criteria-3: Overall cost.

CHALLENGES OF GAN SEMICONDUCTOR DEVICES BASED ON DEVICE CHARACTERISTICS

Three different types of GaN semiconductor power devices are available on the market today. All of them are based on HEMT (High Electron Mobility Transistor), and are lateral transistors. Those are, a) normally-on (or depletion-mode), b) cascode, and c) normally-off (or enhancement-mode) devices.

Normally-on GaN is intrinsically "on" when gate is biased zero. It has very high mobility and zero reverse recovery capacitance which is preferable for high frequency switching. However, normally-on devices do not meet Criteria-2, mentioned above. Vth is around -10V and require less than -15V to turn off. "On" at zero gate bias is fatal for power conversion applications, and power electronics engineers need to put great effort to design circuitry and special gate control to guarantee safety. Moreover, extra circuitry results in larger gate loop which increases parasitics. Special power supply (negative voltage source), additional components and larger PCB reflect to cost. As such, it cannot realize high-efficiency, high-power density, and low noise.

Cascode GaN devices have been introduced to solve the normally-on problem. In this solution, normally-on GaN HEMT devices are connected in series to Si low-voltage MOSFET (LVMOS). The source terminal of the LVMOS device is connected to the gate terminal of normally-on GaN and implemented in a package. In this configuration, the LVMOS drives the GaN device and threshold voltage becomes positive. A commercial gate driver could be used with little additional development from the power electronics engineers leading to less overall cost. However, Criteria-1 is compromised since overall performance is determined by the reverse recovery capacitance and additional on-resistance of LVMOS. Similar configurations with LVMOS in series, but to separately control GaN and LVMOS, such that LVMOS is switched only at the power-up or power-down, is also proposed [4]. This mitigates the performance problem, but drawbacks include special drivers, additional components, a power supply, and sophisticated control..

Normally-off GaN devices are expected to be the ultimate solution to meet all three criteria. Current commercially available normally-off GaN has a p-GaN gate, where p-type GaN is formed on top of HEMT structure to shift Vth [5]. The structure is equivalent to a back-to-back diode which minority carriers (holes) are required in operation which may not provide the best performance. Sensitivity to over-voltages is an issue for p-GaN HEMT which requires sophisticated control to keep proper operation. An improved version of p-GaN called hybrid-drain embedded gate injection transistor is also available at the market. Zero recovery capacitance is maintained, and on-resistance is less affected compared to cascode devices. This provides performance benefits if it is switched around mega-hertz frequencies or less. Although Vth is shifted to positive voltage, it is less than 2V, which is just shy of what power electronics engineer desires. Vth margin is low and still susceptible to gate-to-source voltage fluctuations to cause erroneous turn-on. Moreover, since this device is usually driven by a current source, a dedicated gate driver is required [6]. In addition, there are still some reliability issues remaining such as instability due to trapped charges leading to current collapse and increase of gate leakage current.

As summarized in Table I, normally-off p-GaN device could be the best option currently. However, there is no definitive GaN power semiconductor device which brings out the potential Baliga predicted and fulfills major criteria for power device selection. To overcome this situation, there could be a couple of different approaches. One is to introduce different device structure based on different concept to achieve higher Vth, while maintaining low on-resistance and low capacitance. If this approach succeeds, it would be much easier for power electronic engineers to consider GaN as a candidate to replace Si. Another direction could be integrating GaN devices with driver circuits in the same package. This minimizes parasitics and mitigates power electronics engineer's effort to make use of low Vth power devices. In this approach, answering multiple supplier strategies of the customer would be problematic. In addition, establishment of reliability assessments based on material science and device physics is inevitable and unmet.

TABLE I
COMPARISON AMONG COMMERCIALIZED GAN DEVICES

	Normally-on	Cascode	Normally-off
Criteria-1 (Ron, C)	+ +	- -	+
Criteria-2 (Vth)	- - (-10 to -15 V)	+	+/- (< 2V)
Criteria-3 (cost)	- -	+/-	- (dedicated driver)

CONCLUSIONS

While GaN power devices are already commercialized and expansion of the market is expected, challenges to accommodate power efficiency, power density and electromagnetic interference noise remain. Reducing parasitic inductances is key, but it is revealed that commercialized GaN devices requires additional circuitry to drive the gate due to its low Vth leading to increases in parasitics and cost. One direction could be to development new devices which enable higher Vth or to find a packaging solution for the GaN power semiconductor and gate driver which minimizes parasitics.

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ACRONYMS

PKG: Package
PCB: Printed Circuit Board
SDG s : Sustainable Development Goals
AC : Alternating Current
MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor
LVMOS: Low Voltage MOS