Drift Region Epitaxy Development and Characterization for High Blocking Strength and Low Specific Resistance in Vertical GaN Based Devices

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Abstract

We demonstrate parallel plane junction (avalanche) and punch through one dimensional *pn*-diodes grown on sapphire substrates and compare the results to the GaN breakdown voltage values as a function of the drift region doping concentration. For this demonstration, five different GaN on sapphire substrates with different drift region doping concentrations were grown. A power figure of merit of 1.43 GW / cm^2 is observed for quasi-vertical GaN on sapphire *pn*-diodes with a drift region thickness of 5 µm and a doping of 1.2 × 10^{16} cm^{-3}. These *pn*-diodes demonstrated an excellent blocking performance with hard breakdown at 920 V and a specific drift region resistance of 0.57 mΩ·cm^2.

INTRODUCTION

Lateral GaN heterojunction transistors (HEMT) have only lately entered the low voltage consumer applications thanks to benefits from their low losses and high switching frequencies, however, for high power applications such as high-power converters in the automotive and energy industry, lateral devices have some inherent drawbacks including limited device scaling, low blocking voltage, poor thermal power distribution and dissipation.

Vertical GaN based power switching devices, diodes and transistors, on the other hand, are particularly desirable in those fields due to their reduced die size in comparison to lateral heterostructures based devices. This results in a reduction of specific ON state resistance, $R_{ON} \times A$, by one order of magnitude down to 1.0 mΩ·cm^2 [1-4]. Also, the vertical device concept allows for aggressive device scaling, in respect to gate periphery length per area, and enables high current densities per unit area. The targeted blocking capability larger than 1 kV demands the growth of drift layers thicker than 10 µm with low residual background doping.

However, the drift region conductivity, in particular for thick n$^-$-GaN drift layers, may be limited by low mobility, low carrier density, back ground compensating doping, high defect density and built in potential barriers, having a direct impact on the device electrical performance.

Further, high manufacturing costs and limited production scale for high quality GaN substrates further limits the advancement for GaN based devices.

Cheap alternatives do exist in foreign substrates for GaN layer growth and subsequent substrate removal, however, epitaxial growth of thick GaN layer on foreign substrates only gets harder. The thermal expansion coefficient mismatch between the GaN epi layers and the foreign substrate results in strained GaN layers and in large wafer bow.

That is a key issue for manufacturing, to the point that GaN-on-Silicon, GaN-on-Sapphire and GaN-on-SiC all have a limited total thickness for the GaN layers that can be grown and safely processed.

In order to design high voltage devices, GaN layers needs to be properly engineered, with constant optimization feedback between processing and material development.

Previously, we provided a direct evaluation method for the conductivity properties of low carrier density n$^-$ GaN drift regions with a fast feedback loop to the epitaxy grower that is required in order to reduce the innovation cycle time and speed up the optimization process [5].

Nevertheless, the blocking strength of the drift region must be demonstrated. Schottky diodes under reverse bias may be used for this evaluation, but they may suffer from intense reverse conductance as a result of the Schottky barrier lowering through deep trapping levels and edge termination limitations [6]. *pn*-diodes, alternatively, are a useful tool for the same purpose [7-20]. However, they require GaN:Mg *p*-type layer regrowth on top of the drift region, additional in situ activation and a de-hydrogenation process step. In this work, we assess the n$^-$-GaN drift region properties in terms of forward bias conductivity and revers bias blocking strength for thick n$^-$ GaN layers with different doping concentrations.

DEVICE FABRICATION

We target parallel plane junction (avalanche) and punch through one dimensional *pn*-diodes on sapphire substrates in order to compare the results to the GaN theoretical breakdown voltage values as a function of the drift region doping concentration [7].

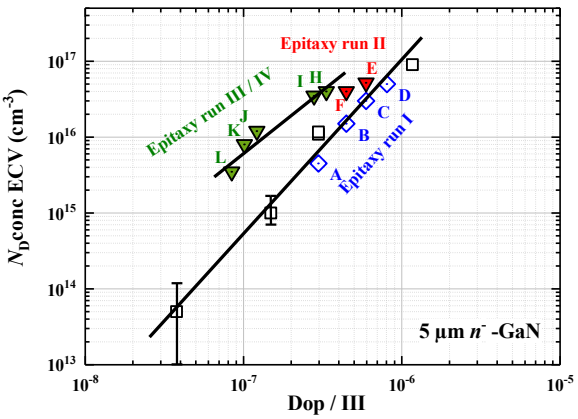

Fig. 1. Carrier density concentrations measured by Electrochemical CV (ECV) as function of the ratio of the molar flows of the dopants to the group III precursors on different GaN on sapphire wafers. Epi runs I and II data is taken from [5].

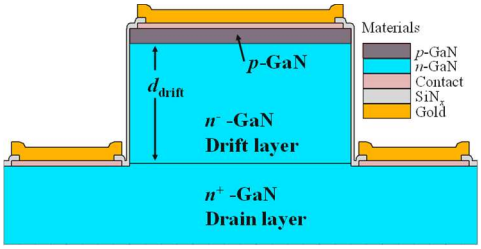

Fig. 2. Schematic cross section of the quasi-vertical *pn*-diode

For this demonstration, five different GaN on 100 mm sapphire substrates with different drift region doping concentrations were grown.

The epitaxial layers are grown by metalorganic vapor phase epitaxy (MOVPE). The epitaxial stack consists of a 2.2 µm unintentionally doped GaN buffer layer, a 2.4 µm n^+ GaN:Si (N_D = 3.0 × 10^{18} cm^{-3}) highly conductive drain layer and a 5 µm n^- GaN:Si drift layer with different doping concentrations from N_D = 3.5 × 10^{15} cm^{-3} to 4 × 10^{16} cm^{-3}, see details in table I.

The drift layer doping concentration is confirmed by electrochemical capacitance voltage (ECV) measurements (see figure 1). A 500 nm GaN:Mg 1 × 10^{19} cm^{-3} layer with additional 30 nm GaN:Mg 2 × 10^{19} cm^{-3} contact layer are regrown and in situ activated in a separate MOVPE reactor. The main difference between run I and run II shown in figure 1 consist in a variation of coalescence time and thickness, 2.0-2.4 µm, of the undoped GaN buffer.

In run II a slightly faster coalescence after nucleation in conjunction with a prolonged growth time of the undoped buffer led to an improved GaN surface morphology [5]. In run III and IV a higher V/III ratio used during drift layer growth resulted in a slightly higher background doping probably due to a lower carbon incorporation.

The device manufacturing process sequence starts with the p-type GaN de-hydrogenation in a rapid thermal annealing furnace. Next, the mesa structures are defined by optical lithography and the surrounding GaN layers are etched down by chlorine based inductively coupled plasma (ICP) dry etching process to the lower highly conductive drain layer. In selected areas, only the *p*-GaN layer is removed to allow contacts directly on the drift layer.

Then, top side *p*-type and *n*-type ohmic contacts are formed on the *p*-GaN and on the drift region, respectively. Additional lower side *n*-type ohmic contacts are formed on the highly conductive drain layer for quasi-vertical configuration measurements. After the mesa edges are wet treated with 25% TMAH, the device is passivated with 200 nm PECVD-deposited SiNx, to avoid leakage currents, the sidewalls are exposed to NH_3 plasma for 15min in situ before the passivation.

All ohmic contacts are reinforced with 1 µm evaporated Au to form contact pads. For high voltage measurements the devices are additionally passivated with 10 µm of Benzocyclobutene (BCB).

The processed pn-diodes schematic cross section is depicted in Fig. 2.

TABLE I
EXPERIMENTAL WAFERS EPITAXIAL STRUCTURE, WAFERS' LEVEL MEASURED DRIFT REGION AREAL SPECIFIC RESISTANCE AND BREAKDOWN VOLTAGE.

Wafer	*p*-GaN	Drift	$(R_{ON}×A)_{drift}$ (Ω cm^2)	V_{BR} (V)
"H"	500 nm GaN:Mg ~1 × 10^{19} cm^{-3}	5 µm GaN:Si 4 × 10^{16} cm^{3}	3.3 ± 0.5 × 10^{-4}	540
"I"	500 nm GaN:Mg ~1 × 10^{19} cm^{-3}	5 µm GaN:Si 3.5 × 10^{16} cm^{3}	3.6 ± 0.6 × 10^{-4}	600
"J"	500 nm GaN:Mg ~1 × 10^{19} cm^{-3}	5 µm GaN:Si 1.2 × 10^{16} cm^{3}	5.7 ± 0.4 × 10^{-4}	920
"K"	500 nm GaN:Mg ~1 × 10^{19} cm^{-3}	5 µm GaN:Si 0.8 × 10^{16} cm^{3}	6.7 ± 1.0 × 10^{-4}	875
"L"	500 nm GaN:Mg ~1 × 10^{19} cm^{-3}	5 µm GaN:Si 3.5 × 10^{15} cm^{3}	1.4 ± 0.2 × 10^{-3}	965

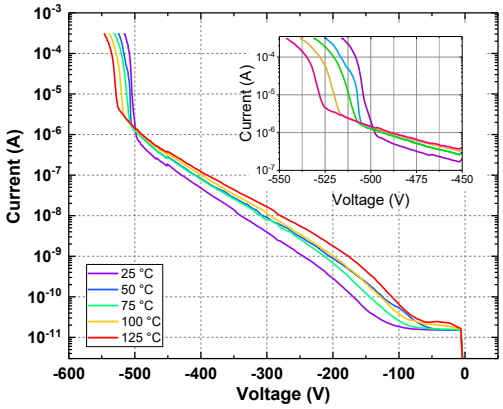

Fig. 3. Reverse bias IV characteristics of wafer “H” as function of the temperature.

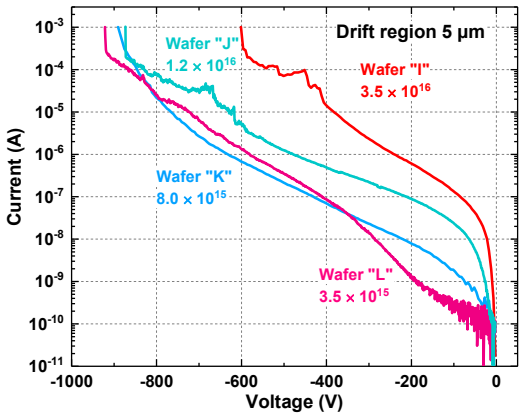

Fig. 4. Reverse bias IV characteristics measured on Wafers ”I”-“L”.

Device Characterization and Analysis

The drift region specific resistance $(R_{ON}\times A)_{drift}$ and breakdown voltage V_{Br} is assessed and summarized for all samples in table I. $(R_{ON}\times A)_{drift}$ decreases monotonically with increasing drift zone doping concentration, N_D, but there is no monothonical relation between V_{Br} and N_D.

pn-diodes manufactured on wafer “H” with high N_D experience non-destructive exponential increase of the reverse current above 500 V (see fig. 3).

Further, repetition of the measurement at elevated temperatures up to 125°C shows an increase of V_{Br} with temperature. This indicates one-dimensional parallel plane junction avalanche conditions for this wafer.

Diodes manufactured on wafers “I” to “L” with lower N_D experienced a non-avalanche hard breakdown and do not scale well with N_D. (Fig. 4). This suggests a shift from the parallel plane junction avalanche regime to the punch through breakdown limit, when reducing N_D. A good fit to the empirical model presented by Maeda et al.[7] was found, see

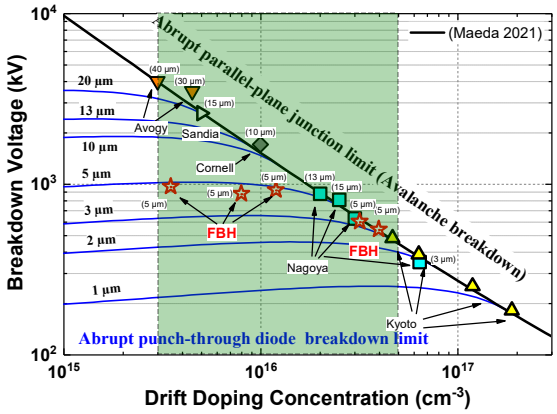

Fig. 5. Quasi-vertical *pn*-diodes breakdown voltage as function of the drift region carrier concentration. The one-dimensional breakdown empirical charts are calculated from [7]. The green band indicates the drift region specific resistance target.

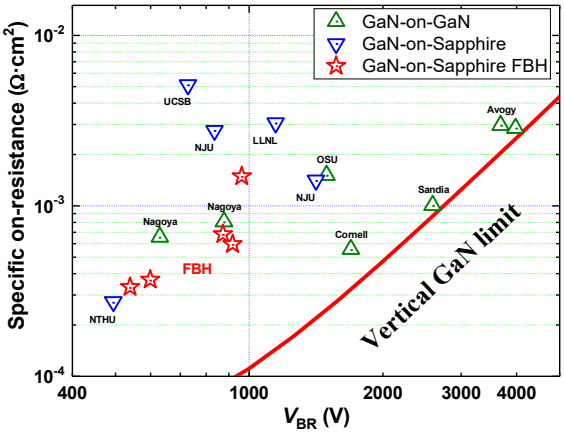

Fig. 6. *pn*-diodes breakdown voltage as function of the drift region specific resistance $(R_{ON}\times A)_{drift}$. Reference values are taken from [8-21]

Fig. 5. where the results are also compared to best reported avalanche breakdown GaN-on-GaN *pn*-diodes.

The results are summarized on the power plane diagram in figure 6 and compared to state of the art reported GaN on sapphire and GaN on GaN quasi-vertical *pn*-diodes. A power figure of merit (PFOM) of 1.43 GW / cm^2 is demonstrated for quasi-vertical GaN on sapphire *pn*-diodes on wafer “J” with a drift region thickness of 5 µm and a doping of 1.2×10^{16} cm^{-3}. These *pn*-diodes obtained an excellent blocking performance with hard breakdown at 920 V and drift region specific resistance of 0.57 mΩ·cm^2.

The PFOM was also optimized to be the highest possible for a 5 µm thick GaN drift zone within the given limitation of the device concept. Details of the optimization procedure and theory are explained in our recent paper [8].

CONCLUSIONS

We report on the recent advancement of our team in the technology for GaN on sapphire drift layer growth capability and quality, while also showing the results obtained with an effective feedback loop between processing scientist and epitaxial grower, smart design and proper characterization techniques.
We were able to produce vertical *pn*-diodes with over 900V blocking voltage and as low as 0.33mΩ cm^2, which competes with other state of art GaN devices for the highest PFOM reported.

ACKNOWLEDGEMENTS

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ACRONYMS

HEMT: High Electron Mobility Transistor
MOVPE: Metalorganic Vapor Phase Epitaxy
ECV: Electrochemical Capacitance - Voltage
ICP: Inductively Coupled Plasma
IV: Current-Voltage
PFOM: Power Figure of Merit