Scalable Manufacturing of Planar, Large-Area 1.2kV and 3.3kV Vertical GaN PiN Diodes

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Abstract

A pilot production scale manufacturing process developed at NRL for planar vertical GaN PiN diodes is presented. Process modules include optimization of p-ohmic and back side n-ohmic metals, as well as a novel hybrid edge termination utilizing nitrogen implants to control conductivity in p-GaN epi layers. Techniques for incoming metrology and mapping processes, as well as auto probe mapping of device performance and yield analysis, are also shown.

INTRODUCTION

GaN-based power switching devices are of significant interest for high efficiency power conversion circuits in medium voltage applications. In particular, vertical GaN device technology is rapidly maturing with the widespread availability of 50mm diameter free-standing GaN wafers. However, there are still significant challenges preventing mass production and widespread adoption. In particular, the relationship between substrate specifications and device performance is not well understood, ion implantation technology for selective-area p-type doping is not reliable, and device failure mechanisms are poorly understood due to a lack of large data sets from electrical stressing [1-3]. To address this challenge, we have established a pilot production scale manufacturing process for vertical GaN diodes on 50mm wafers. This process includes a comprehensive study of incoming metrology and wafer mapping, the development of a fully planar device process for diodes scaled to be capable of practical voltage and current levels (10A, 1.2kV target) including ion implanted edge terminations, and auto probe mapping of device performance following fabrication. By producing large quantities of devices (>500 devices per wafer) and comparing incoming metrology to device performance, we are able to establish pass/fail criteria for incoming epitaxial layers and directly probe the effect of substrate and epi defects on device performance. In addition, by holding the process constant we are able to directly probe the effect of scaling to large area devices as well as scaling epitaxial layers for higher voltage operation (i.e. 3.3kV)

EXPERIMENTAL

The epitaxial PiN diode layers were grown by metal organic chemical vapor deposition (MOCVD) on 50mm commercially available GaN wafers. The 1.2kV diode design had a drift layer design of 8um/1E16cm^{-3}, while a second generation 3.3kV design was 25um/4E15cm^{-3}. The anode design was experimentally varied from 300-500nm, and doping was evaluated from 3E17 to 2E19 cm^{-3}. Incoming metrology includes C-V mapping using a Hg probe to calculate doping and uniformity, optical profilometry, and XRD mapping. The results of C-V mapping are shown in Fig 1. The optical profilometry data is analyzed using a machine learning algorithm to identify bumps, pits, and regions of high roughness. We have previously correlated substrate features to device behavior using arrays of devices specifically aligned to the substrates [4-6]. Using this data, we can predict yield of a given wafer using a machine learning algorithm, which continues to be trained using new experimental data. An example is shown in Fig. 2

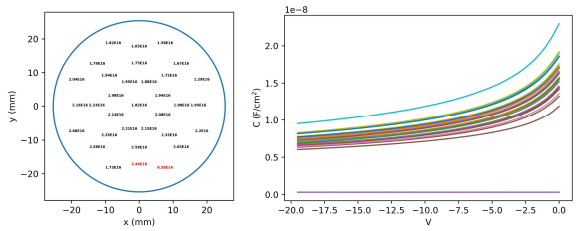

Fig. 1. C-V Mapping curves and analyzed map

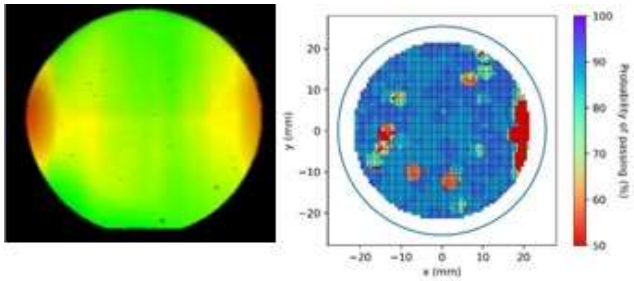

Fig. 2. Optical profilometry map & extracted yield prediction

Following metrology, the wafers are cleaned, and then the edge termination is processed utilizing a multi-step N implant in a box profile to 1) isolate the devices through the p-GaN layer, and 2) form the edge termination region utilizing a hybrid structure consisting of a junction termination extension (JTE) region with guard rings (GR) superimposed via a spacer layer, which has been shown in simulation to approximate a shallow angle bevel, discussed later. Following cleaning processes, both front side p-ohmic metal and back side n-ohmic metal are deposited. A device cross section and optical image is shown in Figure 3.

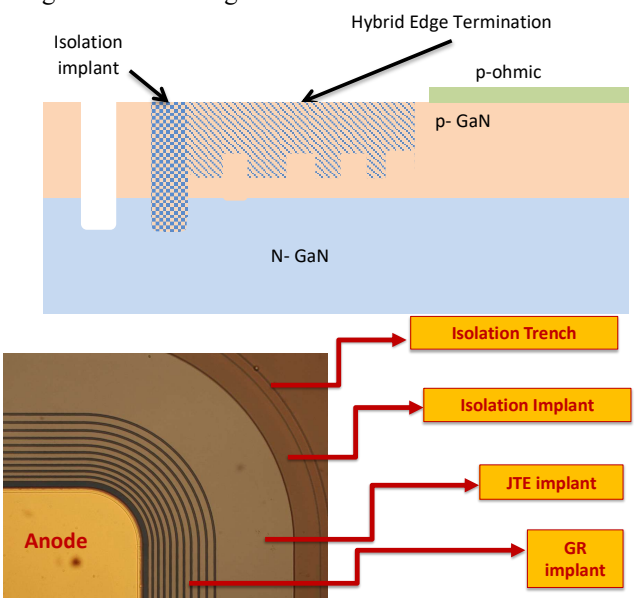

Fig. 3. Device Cross-Section and Optical Image

The wafers are tested under DC and pulsed forward I-V, resulting in maximum current of 18A for a 1mm^2 device and on-resistance of 1.2 mOhm-cm^2. C-V mapping is also implemented to confirm the initial metrology. Reverse I-V is captured both in an auto probe measurement as well as manually in order to collect electroluminescence data to validate the edge termination process. Finally, selected devices are evaluated in depth using electroluminescence imaging and electrical stress testing.

Results & Discussion

Typical forward and reverse I-V data, compiled for a full wafer of devices, is shown in Fig. 4. As observed on the forward data, the devices exhibit a highly uniform turn-on behavior, with low leakage current and high current capability. This is indicative of a high quality p-n junction and relatively few pinholes in the film. However, this distribution is, of course, correlated to incoming wafer properties. While results are shown on an exceptional wafer, we have also observed many devices with premature turn-on on inferior wafers. We have identified the cause of this to be pinholes in the epitaxial layer, causing a short of the anode metal to the substrate, caused by particles introduced during epitaxial growth. Breakdown voltage of up to 1.4kV was observed, with leakage current <1nA at up to 1kV for the 8um drift layer design. Again, this represents the best performing discrete device. As shown on the right side of Fig. 4, there is a very broad distribution of breakdown behavior, even on what is considered a high-quality wafer. Many devices exhibit high leakage current, or a transition to a high leakage state at ~50% of breakdown. The mechanism for this is yet to be determined, but we speculate that it could be the result of localized variations in the drift layer properties due to miscut variation or epitaxial defects. For the 25um epi design, we observed breakdown voltage up to 3.8kV with leakage current <1nA to 3kV for the 25um epi design, as shown in Figure 5.

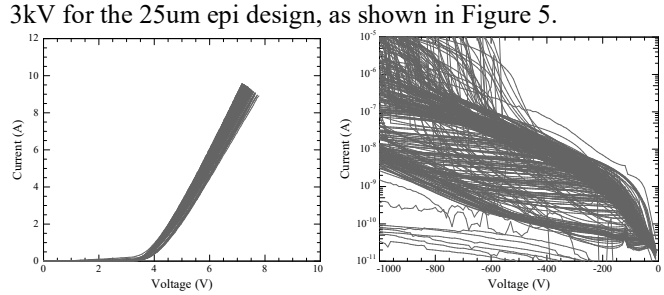

Fig. 4. Forward and Reverse I-V data from a single wafer

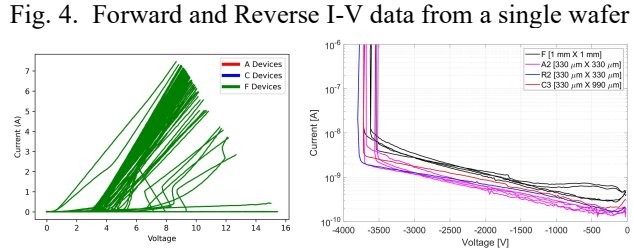

Fig. 5. Forward and Reverse I-V data from a 3.3kV wafer

Optimization of edge termination design is critical to achieve abrupt, avalanche breakdown. To study this, we developed a controlled experiment to implement in the production process. By varying the anode thickness, we were able to systematically vary the thickness of the remaining p-GaN layer, since the implant depth is constant and the wafers are processed in parallel. In doing so, we observed that by making the anode thin, and thus the underlying p-GaN layer constituting the JTE/GR region <10nm, we were able to achieve >100X reduction in leakage current under reverse bias conditions. In addition, temperature-dependence of the reverse I-V behavior changed to show an increased breakdown voltage at elevated temperature. Finally, we also observed the electroluminescence spot moving from the edge of the isolation implant to the edge of the anode. The latter two observations are consistent with avalanche breakdown.

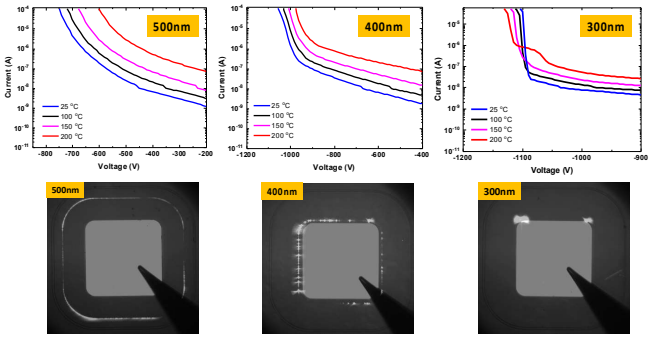

Fig. 5. Edge termination design and optimization

In addition to understanding device behavior and developing processes suitable for multi-wafer fabrication processes, an important aspect of this program is device evaluation and statistics. As such, we have developed automated probing algorithms to test I-V, C-V, and reverse I-V on-wafer, extract relevant device parameters such as on-resistance, maximum current capability, turn-on voltage, ideality factor, leakage current, drift layer doping density, and breakdown voltage. An example of a set of maps from a single wafer is shown in Fig. 6. This is essentially a visual representation of the data discussed above in Figure 4, but we are now spatially correlating the data allowing an evaluation of uniformity within wafer. By viewing the data this way, new insights can be observed. In particular, we can observe a gradient in the reverse leakage current in the lower half of the wafer. This represents the set of devices that have high breakdown voltage, but transition to a high leakage state. We can thus focus on this region of the wafer with detailed evaluation techniques to identify the nature of this behavior.

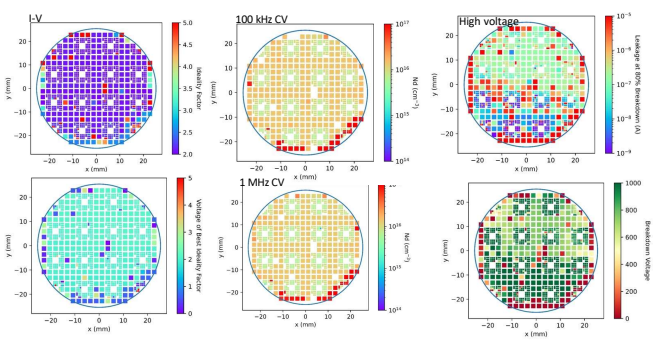

Fig. 6. Auto probe maps of I-V, C-V, and reverse I-V

A second observation from fabricating many wafers and many lots is that there can be substantial variation wafer-to-wafer. As shown in Figure 7, which is a histogram of on-resistance for all 6 wafers in a particular Lot, we can see that several wafers are highly clustered with low resistance, while other wafers have a broader distribution and shifted toward higher on-resistance. Since all wafers were processed in parallel, this is likely due to variations in the epitaxial layers, either drift layer doping or anode doping, or the back side state received from the wafer supplier. Similar trends were observed Lot-to-Lot, though these can be explained by variations in the process maturity and also tracked to the state of process tools.

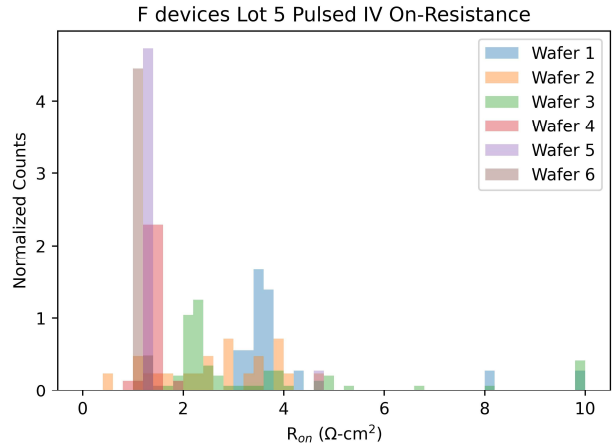

Fig. 7. Histogram demonstrating variability within Lot

Finally, in order to functionally test these devices in a circuit, one must package the devices. We developed a surface mount package process using a commercially available package and outsourced mounting and wire bonding. After packaging, the devices are encapsulated with Hysol. As shown in Fig. 9, there was no device degradation following packaging, and performance typically improved. This is attributed to a passivation effect from the encapsulation material, as there is no passivation process currently employed in the production process.

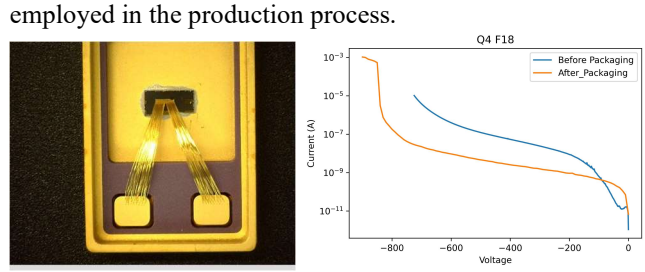

Fig. 9. Device Packaging and I-V Performance

Conclusions

A "pilot production" scale, planar process for vertical GaN PiN diode fabrication has been demonstrated. We have developed process modules for incoming metrology and device evaluation, in addition to device processing. We have identified appropriate edge termination designs for given anode specifications. Yield is highly wafer dependent, but correlated to incoming metrology. A total of 40 wafers have been processed to date, resulting in >20,000 devices. Preliminary work is ongoing to establish packaging processes and develop electrical stress protocols to identify fundamental failure mechanisms.

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