Achieving Application-Reliable GaN FETs Using a Standardized Approach

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Abstract

A standardized or common approach to reliability validation changes the conversation between supplier and customer. For silicon technologies, the conversation is typically focused on the outcome of standardized testing, whereas for newer technologies, the conversation is around whether the device will be reliable for the intended application. Both conversations have similar goals, but a standardized approach is more effective in increasing the adoption of the technology. The gallium nitride (GaN) power industry has invested considerable time and effort on reliability, formed a JEDEC committee and developed several key guidelines including one on switching reliability. This paper describes how TI GaN power devices are assured reliable by using a common approach.

INTRODUCTION

A common approach to reliability based upon guidelines and standards creates a language between suppliers and customers to conduct stress tests, judge their outcomes, and convey reliability metrics. A common approach also reflects credibility, due to the collective industry expertise in developing the methodology. As a result, the conversation focuses on the outcomes of stress-tests vs their adequacy or suitability for the intended application. It also facilitates the benchmarking and second sourcing of technology from different suppliers. The common approach is important for the widespread adoption of a technology.

For silicon technologies, the industry typically follows the JEDEC standard JESD47 [1] and the Automotive Electronics Council standards AEC-Q100 [2] or AEC-Q101. These are longstanding documents, with JESD47 first published in July 1995 and AEC-Q100 in June 1994. These documents specify many tests which may be classified into three categories: device, electrostatic discharge (ESD), and package. These are tests-to-pass, intended to check device "goodness", and are accompanied by accelerated tests-to-failure for calculating lifetimes from relevant failure mechanisms per JEDEC JEP122 [3].

It is not always easy to find industry-wide agreement on a standardized approach for the reliability of newer technologies. The GaN industry has overcome this by investing considerable time and effort. There is now a substantial body of literature, the JEDEC JC70 committee on the topic of Wide Bandgap Power Electronic Conversion Semiconductors, whitepapers from several companies demonstrating good reliability, and several JEDEC GaN guidelines. GaN FETs are now considered reliable and being deployed in commercial, industrial and automotive products. Importantly, the conversation has changed from "Is GaN reliable?" to "What are the steps to validate GaN reliability?" This paper describes the steps, the reasoning behind them, and shows data from applying the methodology to TI GaN.

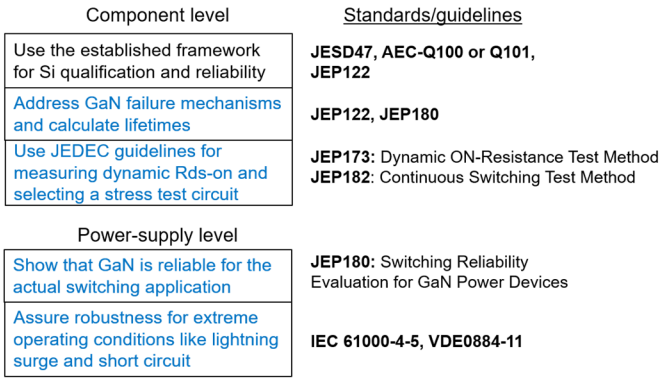

Fig. 1. GaN reliability is validated by GaN specific guidelines in conjunction with established Si standards. The blue text indicates the GaN-specific validation

BACKGROUND

GaN FET reliability is validated through the established Si methodology in conjunction with reliability procedures and test methods developed to address GaN-specific failure mechanisms. The methodology to achieving reliable GaN products is shown in Fig. 1. We have categorized it into component and power-supply level blocks, with the relevant standards and guidelines for each block.

It is to be noted that the traditional silicon reliability methodology does not include stress tests for the actual switching conditions of power management applications [4]. In particular, a large class of power management applications hard-switch, which subjects the power transistors to simultaneous high-voltage and current. Hard-switching creates a significant quantity of hot carriers, so is a different type of stress than off-state or soft-switching. This is relevant

for all power transistors, not just GaN FETs, and therefore is a gap in the Si methodology itself.

The validation methodology in Fig. 1 considers the failure modes and mechanisms of GaN FETs and their structural and material differences from silicon FETs. In planar GaN power FETs, the primary failure mechanisms are Time Dependent Breakdown (TDB), hot-carrier degradation, and charge trapping. TDB is a well-known phenomenon [5] in dielectrics used in silicon FETs, and its modeling is treated in JEDEC publication JEP122 [3]. It occurs due to cumulative high electric-field and is responsible for increased leakage currents and can lead to hard-failure. Hot carrier degradation and charge trapping are also well-known in Si MOSFETs, where hot-carrier stress causes defect generation and charge trapping can cause shifts in parameters like threshold voltage and on-resistance.

An important consequence of charge trapping in GaN FETs is a shift in the on-resistance, $R_{DS(ON)}$ [6,7]. Negative trapped charge repels channel electrons, which results in fewer electrons in the channel. $R_{DS(ON)}$ increases because the number of electrons in the corresponding portion of the channel layer is reduced. Charge can be trapped in the buffer layer, in dielectrics, and at interfaces. Charge trapping can occur due to high drain voltage when the device is off and from hot electrons when switching. The $R_{DS(ON)}$ inclusive of charge trapping is called dynamic $R_{DS(ON)}$. The dynamic nature arises because $R_{DS(ON)}$ recovers as the trapped charge dissipates or de-traps. It is therefore important to evaluate dynamic $R_{DS(ON)}$ at the timescales of switching cycles, which is different from prevailing methods of $R_{DS(ON)}$ measurement. The JC70 committee has thereby developed the publication JEP173 [8] for the measurement of dynamic on-resistance.

As mentioned earlier, the silicon methodology does not include stress tests for the actual conditions of power management applications. In the case of silicon FETs, proxy tests, e.g., hot carrier injection (HCI) and unclamped inductive switching (UIS) are used to check for operational robustness. For GaN FETs, however, the HCI test is not effective due to the electrically-blocking buffer and the UIS test can cause damage. The JC70 committee has thereby developed the publication JEP180 [9] "Guideline for Switching Reliability Evaluation Procedures for Gallium Nitride Power Conversion Devices".

JEP180 provides a common approach for assuring that GaN products are reliable in power conversion applications. Application reliability is assured by demonstrating that the power FET has both the required switching lifetime for the relevant stresses, and it runs reliably under stringent operating conditions in a power supply. The former uses Switching Accelerated Lifetime Testing (SALT) to stress devices to failure and the latter uses Dynamic High Temperature Operating Life (DHTOL) testing. This is analogous to the traditional methodology (JEP122, JESD47) of Accelerated Lifetime Testing (ALT) for static-bias lifetimes, and High Temperature Operating Life (HTOL) for qualification.

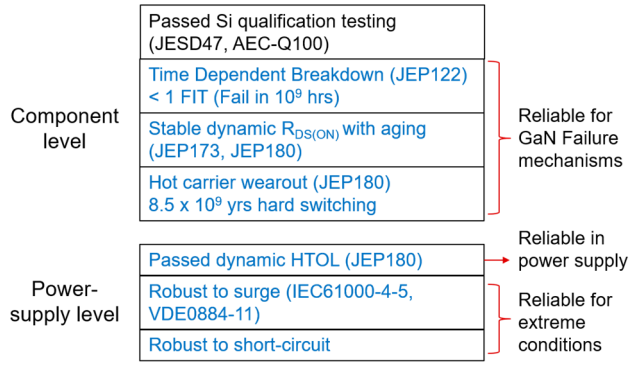

Fig. 2: Reliability testing outcomes for TI GaN corresponding to the methodology shown in Fig. 1. The blue text shows the results of the GaN-specific validation

COMPONENT-LEVEL RELIABILITY

Component-level reliability for TI GaN parts is established by supplementing the traditional Si methodology with the lifetime validation for GaN-specific failure modes and mechanisms. The outcome is summarized in Fig. 2. TI GaN parts are qualified per JEDEC JESD47 for commercial and industrial use, and AEC-Q100 for automotive applications. TI GaN FETs have also been engineered for high TDB lifetime by using special test structures for each of the high-field regions in the device. A model has been built per JEP122 [3], incorporating 1.8 million device hours of testing and shows a low failure-in-time (FIT) rate of 0.8 FIT with 10 years of continuous operation at 480 V and 125°C for the LMG3410R070 product. (1 FIT = one fail in 10^9 device hours of operation)

The power FET also needs to demonstrate good switching lifetime. There are two key failure modes from hot-carrier stress for hard-switching applications: hard-failure from hot-carrier wearout [10,11] and an increase in dynamic $R_{DS(ON)}$. We have run SALT validation per JEP180 to generate a model for switching stress using a hard-switching test-vehicle circuit from JEP182 [12]. The work is described in detail in [11]. JEP180 provides guidelines for broad coverage based upon the switching locus (relevant switching stress) of the application, and our model can calculate the lifetime for any given hard-switching application condition. For example, the LMG3410R070 product has a mean time to failure of 8.5 x 10^9 yrs. for hot-carrier wearout with 400V operation in a power factor correction hard-switching circuit with 1.8 kW output. The very high lifetime shows that parts will not fail due to hot electron wearout for regular operation.

We have also shown that dynamic $R_{DS(ON)}$ is stable with aging. The measurement is conducted per JEP173, using a

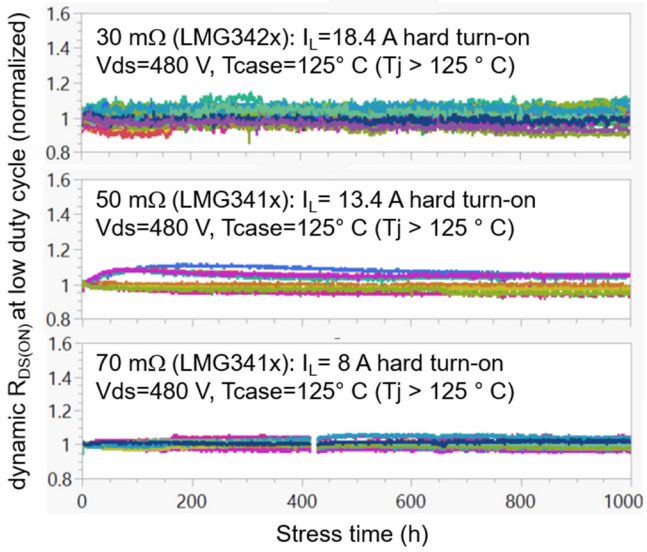

Fig. 3: Dynamic $R_{DS(ON)}$ is stable for harsh low duty cycle hard switching stress showing lack of new trap creation with aging.

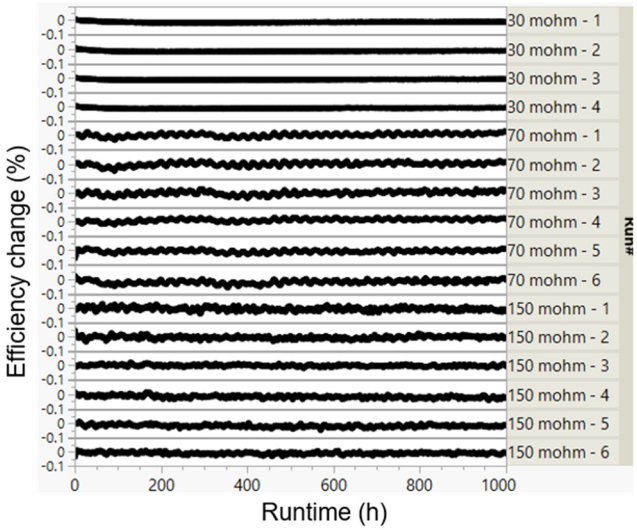

Fig. 4: Parts run stably without failure under JEP180 DHTOL testing, validating good reliability for power supply usage. Parts were run at 480V/125C, 150 kHz, 100 V/ns for 1000h at power levels of: 3.8 kW (30 mΩ), 1.9 kW (50 mΩ), 1.4 kW (150 mΩ.)

hard-switching test circuit from JEP182. The harshness of the hard-switching transition is per the best practice conditions of JEP180. We run the stress at low duty cycle because this stress condition is very effective at validating the stability of dynamic $R_{DS(ON)}$ with aging. Low duty cycle stress provides high trap filling because the device spends most of its time at high-voltage and the small on-time limits de-trapping [7,13]. As a result, it provides an early detection method for trap-related aging by detecting early-stage trap formation. Early-stage latent or nascent traps have lower electrical activity, and may not have an effect on dynamic $R_{DS(ON)}$ with regular (e.g. 50%) duty cycle stress until they age further. The test was run at about 20 kHz with approximately 0.5% duty cycle. Results from the LMG34xx product family shown in Fig. 3. The stable dynamic $R_{DS(ON)}$ validates the excellent material quality by showing that latent traps are not a concern.

POWER-SUPPLY LEVEL RELIABILITY

When parts operate in power supplies, they are subject to additional operating modes than at component-level. For example, in a half bridge, the power FETs operate in dead-time [4] and hard-commutation conditions. This subjects the GaN FET to third quadrant operation and possible reverse-recovery stress. With GaN FETs, one can also reduce the switching loss by increasing the slew rate. High slew-rate switching, however, can cause shoot through or unwanted turn-on of the other FET due to the Miller effect. One also needs to assure the robustness of interactions with the other die in the multi-chip module (MCM), the other half-bridge power device, and with other power-supply components. All the aspects above are addressed by the JEP180 Dynamic High Temperature Operating Life (DHTOL) test.

We run DHTOL testing using half-bridge cards in an H-bridge configuration. The cards are stressed using JEP180 best-practice conditions of maximum recommended voltage, temperature, and power levels and run for 1000 h with parts stressed under both hard- and soft-switching conditions. The parts show stable efficiency and they run without failure, as shown in Fig. 4, which shows DHTOL results on 32 half-bridge cards (64 parts) from the LMG34xx product family from multiple fabrication lots. The stress conditions are listed in the figure caption. Each trellis in Fig. 4 shows the efficiency change of one H-bridge cell (4 parts), calculated from the loss current needed to power the cell. The efficiency remained within 0.1% of its initial value, demonstrating the good system-level reliability of TI GaN products. The result provides confidence that parts will operate stably as they age. This is due to their excellent dynamic $R_{DS(ON)}$ stability shown in Fig. 3. The stable efficiency in DHTOL testing also validates that the switching transition remains clean, without shoot-though effects at high slew rates of 100 V/ns.

ROBUSTNESS TO EXTREME CONDITIONS

Devices also need to be reliable during occasional extreme conditions such as line surge and short-circuit events seen by power supplies operating in the field. Surge robustness has traditionally been assured through the avalanche property of Si FETs. GaN FETs have not yet demonstrated avalanche robustness, so it is important to assure that GaN power supplies will be robust to line surges under the conditions of actual operation. Unlike Si power FETs, GaN FETs have a transient overvoltage margin that allows them to switch through power line surges.

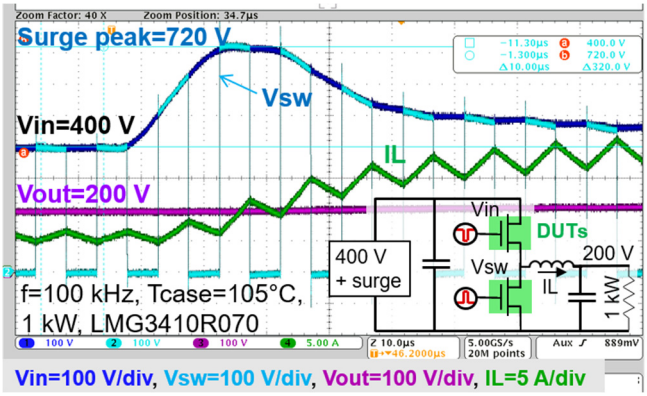

Fig. 5: Surge waveforms, showing the test point parameters of the schematic (inset). The switched node waveform is overlaid on the input waveform to show switching through the surge strike.

We validate surge robustness by subjecting a loaded power supply running half bridges to stringent line surge [6,14]. Surge strikes are applied per the IEC61000-4-5 standard with the peak voltage at the switching FETs reaching 720V. The waveforms and schematic for the surge robustness validation of the LMG3410R070 are shown in Fig. 5. Our test condition is stringent because simulations show that even for a severe surge condition of 4 kV, it is straightforward to limit the voltage seen by the device to 600 V [14]. The available headroom can make GaN based solutions more reliable than Si solutions by providing margin for the degradation of the surge suppression circuitry with aging.

We applied 50 strikes per VDE0884-11, plus another 50 strikes for margin to a half bridge operating at V_{DS} = 400 V, 100 kHz, 50% duty cycle, and delivering 1 kW of power with a case temperature of the hard-switching device at 105°C. The switched node waveform is overlaid on the input waveform to show the switching transitions. An increase in the inductor current from 5 A to 20 A is also seen, further validating the robustness. The use of a half-bridge allows the validation of all modes of device operation under both voltage and subsequent current surges: hard switching, soft switching, blocking, third quadrant operation and hard commutation. The test does not cause hard-fail or efficiency degradation, demonstrating that TI GaN parts are surge robust.

TI GaN parts are also robust to short-circuit conditions. The package-level integration of the driver and protection circuitry using a low-inductance leadframe allows fast detection and turn off within 100 ns [15].

Conclusions

With the industry development of a standardized approach to GaN reliability, a methodology may now be followed to validate if GaN parts are reliable for a given application. GaN FET reliability is validated through the established Si methodology in conjunction with JEDEC reliability procedures and test methods developed to address GaN-specific failure mechanisms. We have shown that TI GaN is reliable for a broad range of application-use by following this methodology. At the component level, parts pass Si qualification testing, have low FIT rates of less than one for time dependent breakdown, show stable dynamic $R_{DS(ON)}$ with aging and will not fail due to hot-electron wearout. At the power supply level, parts pass JEP180 DHTOL testing, showing robustness to stresses seen under power supply operation. Parts are also robust to occasional extreme conditions of surge and short circuit.

Acknowledgements

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References

1. JEDEC Standard JESD47K, “Stress-Test-Driven Qualification of Integrated Circuits”, Sept 2017
2. AEC-Q100, Rev. H, “Failure Mechanism based Stress Test Qualification for Integrated Circuits,” Sept. 2014
3. JEDEC Publication JEP122H, “Failure Mechanisms and Models for Semiconductor Devices”, Sept 2016.
4. S. R. Bahl, D. Ruiz and D. S. Lee, "Product-level reliability of GaN devices,"*IEEE International Reliability Physics Symposium (IRPS)*, 2016, pp. 4A-3-1-4A-3-6, doi: 10.1109/IRPS.2016.7574528.
5. J. W. McPherson, “Brief History of JEDEC Qualification Standards for Silicon Technology and Their Applicability to WBG Semiconductors”, *IEEE International Reliability Physics Symposium (IRPS)*, 3B.1-1, 2018.
6. S. R. Bahl, “Achieving GaN Products with Lifetime Reliability”, available at https://www.ti.com/lit/wp/snoaa68/snoaa68.pdf
7. J. Bocker, C. Kuring, M. Tannhauser, S. Dickerhoff, “Ron Increase in GaN HEMTs – Temperature or Trapping Effects”, *IEEE Energy Conversion Congress and Exposition (ECCE)*, p. 1975, 2017
8. JEDEC Publication JEP173. Dynamic ON-Resistance Test Method Guidelines for GaN HEMT based Power Conversion Devices, v 1.0, Jan. 2019
9. JEDEC Publication JEP180, “Guideline for Switching Reliability Evaluation Procedures for Gallium Nitride Power Conversion Devices, v 1.0, Feb. 2020
10. A. Ikoshi et al., “Lifetime Evaluation for Hybrid-Drain-embedded Gate Injection Transistor (HD-GIT) under Practical Switching Operations”, *IEEE International Reliability Physics Symposium (IRPS),* p. 4E-2.1, 2018.
11. S. R. Bahl, F. Baltazar and Y. Xie, “A Generalized Approach to Determine the Switching Lifetime of a GaN FET”, *International Reliability Physics Symposium (IRPS)*, Apr. 2020, doi: 10.1109/IRPS45951.2020.9129631.
12. JEDEC Publication JEP182. Test Method for Continuous-Switching Evaluation of Gallium Nitride Power Conversion Devices, v 1.0, Jan. 2021
13. K. Li, P. Evans, and M. Johnson, “Characterization and Modeling of Gallium Nitride Power Semiconductor Devices Dynamic On-state Resistance”, *IEEE Trans. on Power Elec*., v. 33, n. 6, p. 5262, 2018.
14. S. R. Bahl and P. Brohlin, “A New Approach to Validate GaN FET Reliability to Power-line Surges Under Use Conditions,” *IEEE International Reliability Physics Symposium (IRPS)*, 2019, pp. 1-4, doi: 10.1109/ IRPS.2019.8720479.
15. S. Dusmez et al., “Overcurrent Protection in High-Density GaN Power Designs”, TI Application Report SNOAA15, available at www.ti.com/lit/an/snoaa15/snoaa15.pdf