Reliability without Hermeticity (RWoH) Protection for SLCFET Switch Technology

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Abstract

The Superlattice Castellated Field Effect Transistor (SLCFET) has proven to be a high-performance RF switch technology offering low loss and high isolation over a wide bandwidth. In this article we further improve on the released 3S SLCFET process by incorporation of a coating which ensures Reliability Without Hermeticity (RWoH). This coating serves to protect the devices and enable them to work reliably under extreme conditions, without expensive hermetic packaging, as shown by Highly Accelerated Stress Testing (HAST) in accordance with JEDEC standards. Most importantly, this coating maintains the high performance of the switches, which is best exemplified by MMIC data from a Single Pole Double Throw (SPDT) switch showing Insertion Loss <1.0 dB and Isolation>25 dB from DC to 50 GHz. This new coating enables a world class performance switch with improved survivability at a lower cost for DoD systems.

The Superlattice Castellated Field Effect Transistor (SLCFET) has been shown to push performance boundaries in the industry for low loss, high isolation, high RF performance switches over a wide bandwidth [1-4]. The released SLCFET 3S switch process has a demonstrated RF switch figure of merit (FCO) ~1.8 THz [1-3] with recent developments pushing it beyond 3 THz [4]. This performance is driven by the unique 3-dimensional superlattice structure that defines SLCFET. These devices are formed by a 3D gate around the superlattice of AlGaN/GaN Two-Dimensional Electron Gas (2DEG) layers which provides low resistance and high mobility. This 3D gate allows for a more uniform electric field to be applied to turn off the device than would be achieved in a more traditional HEMT device.

An additional improvement to these high-performance devices would be to add reliability without hermeticity (RWoH). A common approach to ensure device reliability under extreme conditions is to hermetically package die, which can be expensive and time consuming at the system level. An alternative, and less costly, approach is MMIC level hermetic sealing using a RWoH coating. In this paper we report results from the development of a RWoH coating for SLCFET devices which removes the need for a hermetic seal when packaging. In addition, the superior RF performance of the SLCFET devices is maintained even with these coatings, which generally negatively impact other technologies.

We present data from several different candidate coatings measured on various SLCFET devices and MMICs, both before and after Highly Accelerated Stress Testing (HAST). We focus on the general impact to device performance for the pre-HAST measurements and on device yield post-HAST. The coatings are divided into two layers; a humidity coating that prevents corrosion and a scratch protect coating that acts as a general protection layer for the devices.

Coating	Humidity Coating Thickness	Scratch Protect Thickness
A	Baseline	Baseline
B	1.6 x Baseline	Baseline
C	2 x Baseline	1.2 x Baseline
D	1.3 x Baseline	1.2 x Baseline
E	2 x Baseline	0.8 x Baseline

Table I: Coatings tested on devices to survive HAST Conditions.

The five different coatings used in this study are outlined in Table I. For each of these coatings either the humidity coating or scratch protect was varied, most significantly in thickness, from a baseline coating used in initial testing. Devices using these coatings, Table II, were then evaluated for their yield after HAST testing as appropriate. These devices include a standard FET, isolated metal-insulator-metal (MIM) Capacitor, Single Pole Double Throw (SPDT) switch MMIC, Single Pole Four Throw (SP4T) switch MMIC, and a Filter MMIC. The testing itself followed JEDEC standard 22-A110[5], where devices are

biased at operating voltage, in this case -14V, for 96 hours under 85% relative humidity and a temperature of 130 °C, with appropriate ramp up and down procedures. The evaluations were also performed per the JEDEC standard, assigning a failure to devices which, post-HAST, had exceeded parametric limits or whose functionality could not be demonstrated. Additionally, a visual inspection was performed both before and after HAST testing, to look for signs of corrosion in active regions of the devices to further ensure devices are correctly assessed.

Device	FET Periphery	Capacitor Area
FET	Baseline	None
Capacitor	N/A	Baseline
SPDT	4 x Baseline	0.3 x Baseline
SP4T	6 x Baseline	None
Filter	80 x Baseline	10 x Baseline

Table II: Devices tested in HAST broken down by comparative active regions of FET periphery and MIM Capacitor area.

In order to evaluate the general impact of the coatings on device performance, electrical measurements were performed pre-HAST. In-line test data from RF reliability devices pre-HAST using coating D, Figure 1, show a minor impact on electrical performance and the value of our figure of merit F_{CO}. The minimal impact on performance is further demonstrated by data from MMICs, Figure 2, showing Insertion Loss <1.0 dB and Isolation >25dB in the DC-50GHz range from SPDT devices. In general, the decrease in device performance is primarily from the change in the local relative permittivity surrounding the devices, which increases with the addition of the humidity coating and scratch protect.

Ultimately the concern is not just about how the coatings impact basic device performance, but how well they protect devices from extreme temperature and humidity. The following data focuses on the yield of devices post-HAST testing and shows the results from both the electrical evaluation, shown in blue, and a total evaluation, shown in red that includes the electrical data and a visual inspection for corrosion in active regions of the devices.

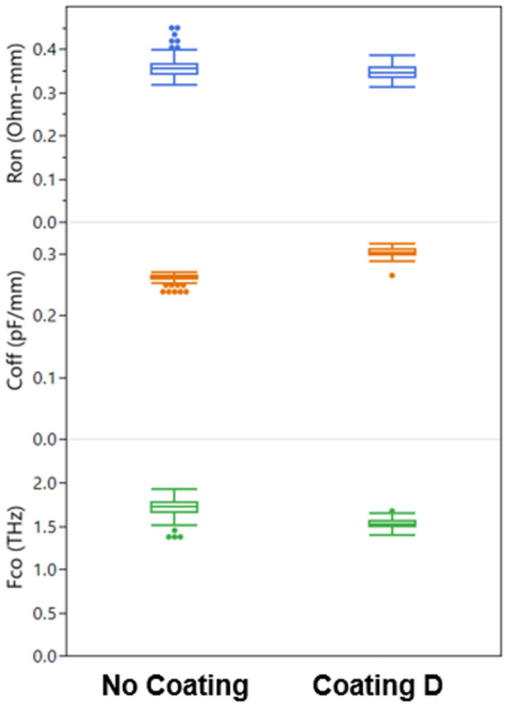

Figure 2: Comparison of inline test data showing impact coating D on Figure of Merit. The coating causes no significant change in R_{ON}, a 15% percent increase in median C_{OFF}, and a 12% decrease in median F_{CO}.

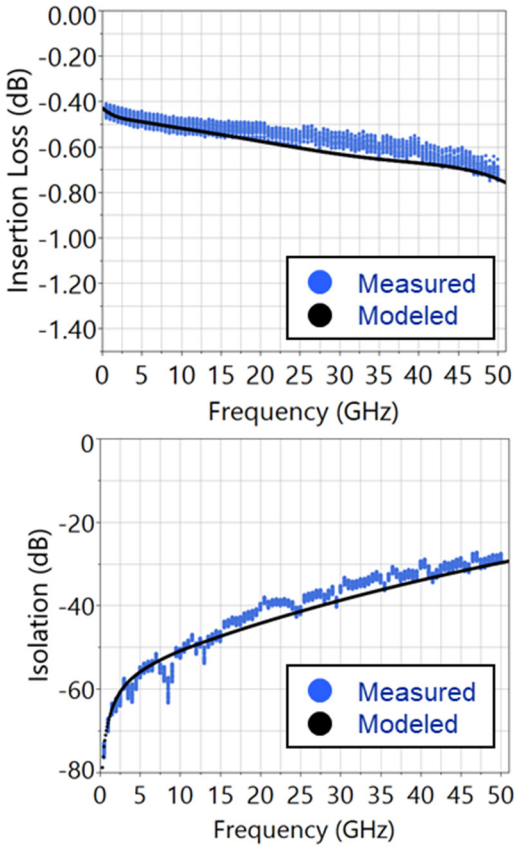

Figure 1: Insertion Loss and Isolation in the DC-50GHz range of a SPDT with the RWoH coating matched to a modeled device.

Initial testing for HAST focused on FET devices, with the results shown in Figure 3(a) for coatings A and B compared to devices with no coating. An electrically passing FET is one that exhibits leakage below 1e-7 A/mm and Ion/Ioff ratios greater than 1e6. Devices with no coating did not yield at all, while devices with the baseline coatings, coating A, showed a 95% electrical yield and a 60% overall yield. To further look at coating viability, SPDT MMIC yield for coatings A and B are shown in Figure 3(b). The SPDTs were evaluated for basic device leakage post HAST, less than 1e-7 A/mm, for the electrical yield, and with the optical corrosion inspection for the overall yield. In this case, coating B performed over three times better than coating A

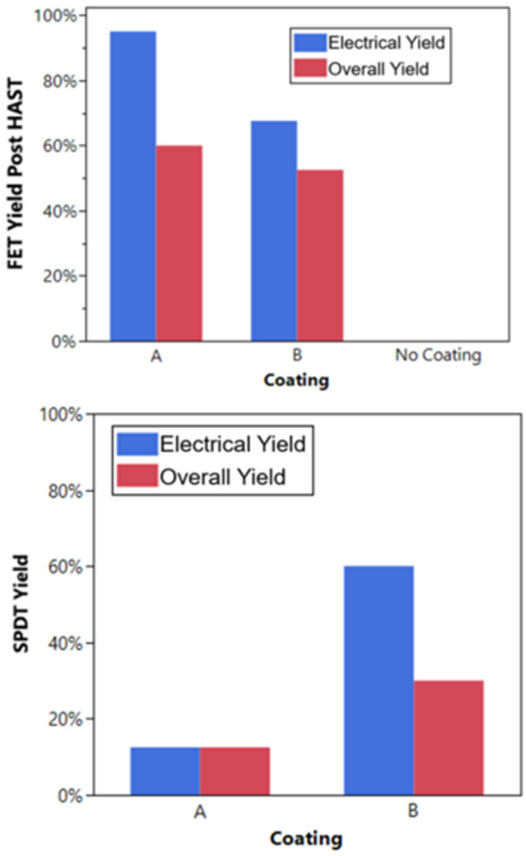

Figure 3: Yield results post-HAST for both FETs and SPDTs using initial coatings. Based on initial test results no SPDTs without a coating were tested as no FET devices without a coating yielded post-HAST.

in electrical yield and over two times better in overall yield. Since the SPDT's had capacitors that were biased in addition to a larger FET periphery, this indicates that a thicker coating may provide better protection on devices that include capacitors as opposed to FET only devices. This was reinforced in the optical inspections which showed the capacitors as the primary failure site. Additionally, this indicates that capacitors may act as a more key metric in evaluating RWoH coatings.

In order to expand upon the initial FET and SPDT results, alternative coatings C, D, and E were used to evaluate isolated Capacitors as shown in figure 4. The

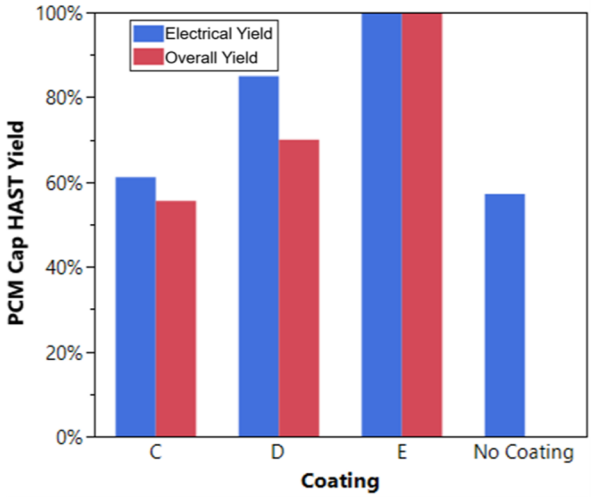

Figure 4: Metal-Insulator-Metal Capacitor Yield post-HAST.

electrical evaluation criterion for Capacitor electrical yield was leakage across the capacitor less than 1e-7 A, and again the overall yield also looked for optical signs of corrosion. The best performing coating on the capacitors was Coating E, showing 100% electrical and total yield. This coating had a thicker than baseline humidity coating and a thinner than baseline scratch protect. Coating D, whose electrical data was shown in Figures 1 and 2, which combined thicker than baseline humidity coating and scratch protect, had an 85% electrical yield, that dropped to 70% when including the optical inspection. The importance of including an optical inspection is shown by the 60% electrical yield of the devices with no coating, as the corrosion was extreme enough to isolate the capacitor plates.

In order to better compare the coating results, the HAST yield results from SPDTs with coatings A, B, D, and E are plotted in Figure 5 using the criteria outlined for Figure 3(b). Similar to the capacitor yield, coating E showed the highest yield at 90% for both electrical and total yield. This again indicates a thicker than baseline humidity coating and thinner than baseline scratch protect provide the best protection of the coatings in this study.

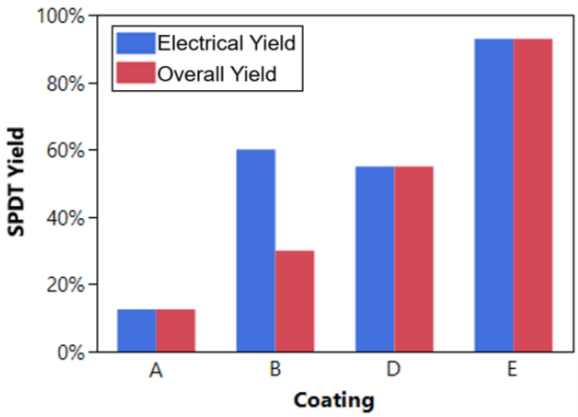

Figure 5: SPDT Yield post-HAST for coatings A, B, D, and E.

To look ahead at potential coating impact on further complex devices, both single pole four throws (SP4Ts) and large-scale filters were tested in HAST with coating D as shown in Figure 6. The electrical criteria being again 1e-7 A/mm leakage, and the additional optical

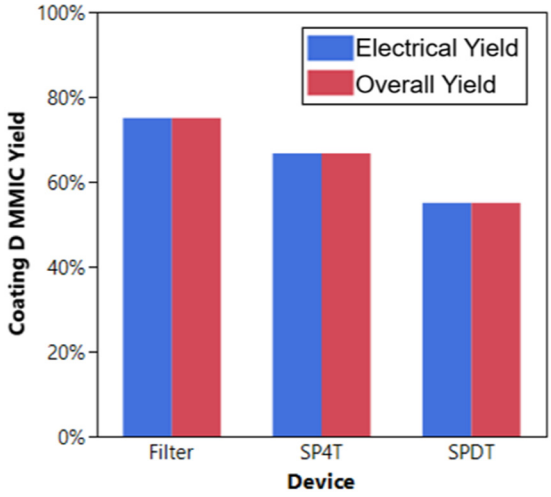

Figure 6: HAST Yield of additional MMICs with coating D.

inspection for the overall yield. The device with the highest yield in this case was the Filter design, showing a slightly higher yield than smaller devices. In this case, the higher yield on the SP4Ts and Filters compared to the SPDT can again be attributed to capacitors. The SP4T does not contain any capacitors. For the Filters, none of the capacitors are biased during HAST testing due to its design. This further indicates the capacitors are a key circuit element in improving our humidity coating. Similar devices with coating E, which had a higher SPDT yield, are currently being tested.

Overall, we have developed a RWoH coating that can protect our standard SLCFET SPDT devices. Additionally, the learning from this work provides a path forward as we evaluate more complex devices. We believe these results continue to show the capability and performance provided by the SLCFET technology with the added benefit of RWoH. The devices maintain their world-class RF performance while gaining a significant boost in survivability and significant cost reduction for DoD systems.

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