Differences in SiC Wafer Thermal Conductivity from Face-to-Face Dependent on Polishing

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***Abstract* – The thermal conductivity of the chemo-mechanically polished Si face and optically polished C face 4H-SiC samples from different suppliers has been examined using transient thermoreflectance. Significantly lower thermal conductivity of the Si face has been observed for higher quality substrates. This is believed to arise from subsurface damage occurring during the polishing process. The impact of the lowering of the near-surface thermal conductivity has been examined for a commercial GaN-on-SiC RF transistor using finite-element analysis.**

I. INTRODUCTION

Single crystal silicon carbide (SiC) is an excellent material for power electronics and as a substrate for GaN-on-SiC RF electronics as a result of its wide bandgap, electrical properties, and high thermal conductivity of between 300 and 420 W m^{-1} K^{-1} [1]. The high thermal conductivity of SiC is especially essential for high power RF transistors to minimise cooling requirements, meaning reduced weight of electronics compared to other semiconductors [2].

An important aspect of SiC growth and processing is the polishing of the different faces. Commonly available commercial SiC substrates have an optical polish on the C back-side whilst undergoing a rigorous chemo-mechanical polish (CMP) on the Si growth face. It is this face which is typically used for epitaxial growth of doped SiC as well as for integration and growth of other semiconductors such as GaN.

Previous work has investigated how different polishing methods can result in different levels and kinds of subsurface damage [3]. These works have shown that, depending on the nature of the polishing, subsurface damage can extend to more than 60 µm below the surface. However, to date there has been minimal characterisation on how these surface preparation techniques affect the thermal conductivity of the SiC substrate. On first sight, one may expect CMP to result in a higher thermal conductivity than coarser polishing techniques, regardless of the SiC vendor.

We have used transient thermoreflectance (TTR) to investigate the thermal conductivity of four semi-insulating 4H-SiC wafers from different vendors on both the Si and C face. Finite element simulations have been used to examine how the different thermal conductivities could affect the thermal management in a GaN RF-transistor.

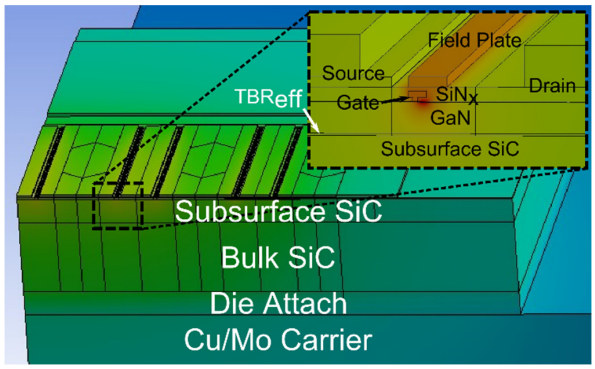

Figure 1. Schematic of the device structure used for finite element simulations. Shown is five fingers of the device which are related by symmetry to the other five. The insert shows the detailed structure of a single finger.

II. EXPERIMENTAL METHODS

The samples investigated are shown in table 1. For TTR measurements, a 150 nm Au transducer was deposited with a 10 nm Cr adhesion layer by thermal evaporation. A 355-nm pulsed laser ($1/e^2$ spot size ~65 µm) was used to heat the surface while a 532-nm continuous wave probe laser ($1/e^2$ spot size ~2 µm) was used to monitor the reflectance change as a function of time. This is linearly proportional to the temperature change of the

Table 1. Details of samples purchased and extracted SiC thermal conductivity. Error is given as the 10th and 90th percentile of the fitted probability distributions from Monte Carlo analysis

Vendor	Si Face Polishing	Si Face Thermal Conductivity (W m^{-1} K^{-1})	C Face Polishing	C Face Thermal Conductivity (W m^{-1} K^{-1})
1	CMP	253±33	Optical	300+42/-43
2	CMP	263+33/-32	Optical	277+49/-40
3	CMP	240±30	Optical	343+45/-44
4	CMP	243±33	Optical	196±31

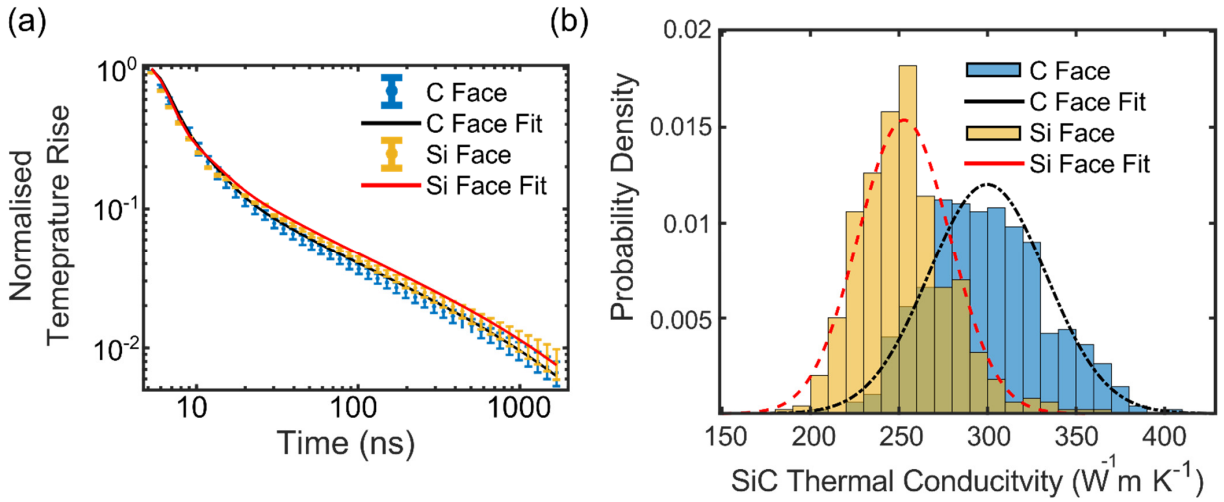

Fig. 2: (a) Examples of fitted thermoreflectance traces for the sample from vendor 1 for the C and Si face; (b) shows the histograms from Monte Carlo analysis for the same sample. The darker colours in the centre indicate overlap of the C and Si face probability distributions.

sample surface. To extract the average isotropic thermal conductivity of the SiC in the first ~ 25 µm, the normalised traces were fitted by solving the heat diffusion equations through a multilayer stack using a global search algorithm with an adapted least squares fitting routine [4]. The fixed parameters are shown in Table 2. Errors were estimated using Monte Carlo error analysis, repeating the fitting 500 times with slight variations in the fixed properties of the materials and the lasers. In addition to fitting the SiC thermal conductivity, the effective thermal boundary resistance between the Au and the SiC was also fitted.

Three-dimensional finite element simulations were carried out to model a ten-finger Cree CGH400010 commercial transistor operating at a power dissipation of 5 W mm^{-1}, varying the thermal conductivity of the first 25 µm of SiC using the values measured in this work. The GaN buffer was 1.4 µm, effective thermal boundary resistance was 15 m^2 K GW^{-1}, gate length was 250 nm, gate width was 350 nm, gate pitch was 40 µm, gate-drain spacing was 2.8 µm, and the drain-source spacing was 4 µm. The structure used is shown in Fig. 1. Appropriate temperature dependencies were used for the thermal conductivity of each material. Parameter response surfaces were generated by varying the subsurface thermal conductivity of the SiC, TBR_{eff}, and GaN buffer thickness. The GaN thermal conductivity had a thickness dependency based on the work of Ziade *et al.* [5].

Table 2. Fixed parameters used for TTR analysis.

Material	Isotropic Thermal Conductivity	Density (Kg m^{-3})	Specific Heat (J Kg^{-1} K^{-1})
Au	200[6]	19320[7]	128[7]
4H-SiC	Fitted	3211[8]	690[8]

III. RESULTS AND DISCUSSION

Examples of fitted thermoreflectance traces and histograms from error analysis are shown in Fig. 2.

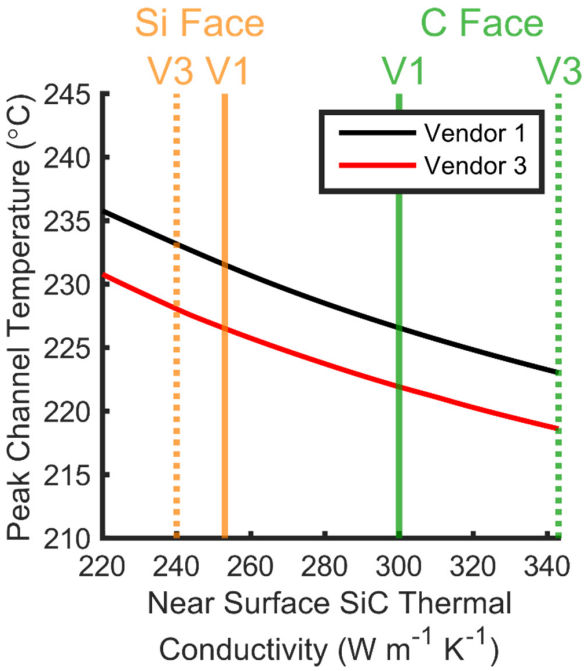

Fig. 3: Simulated peak temperatures for a commercial GaN-on-SiC RF transistor operating at 5 W mm^{-1}. The first 25 µm of SiC thermal conductivity (TC) was varied whilst bulk TC was taken as that measured from the C face for vendor 1 (black) or vendor 3 (red). Vertical lines indicate the measured TC of the Si face (orange) and C face (green) for both vendor 1 (solid) and vendor 3 (dotted).

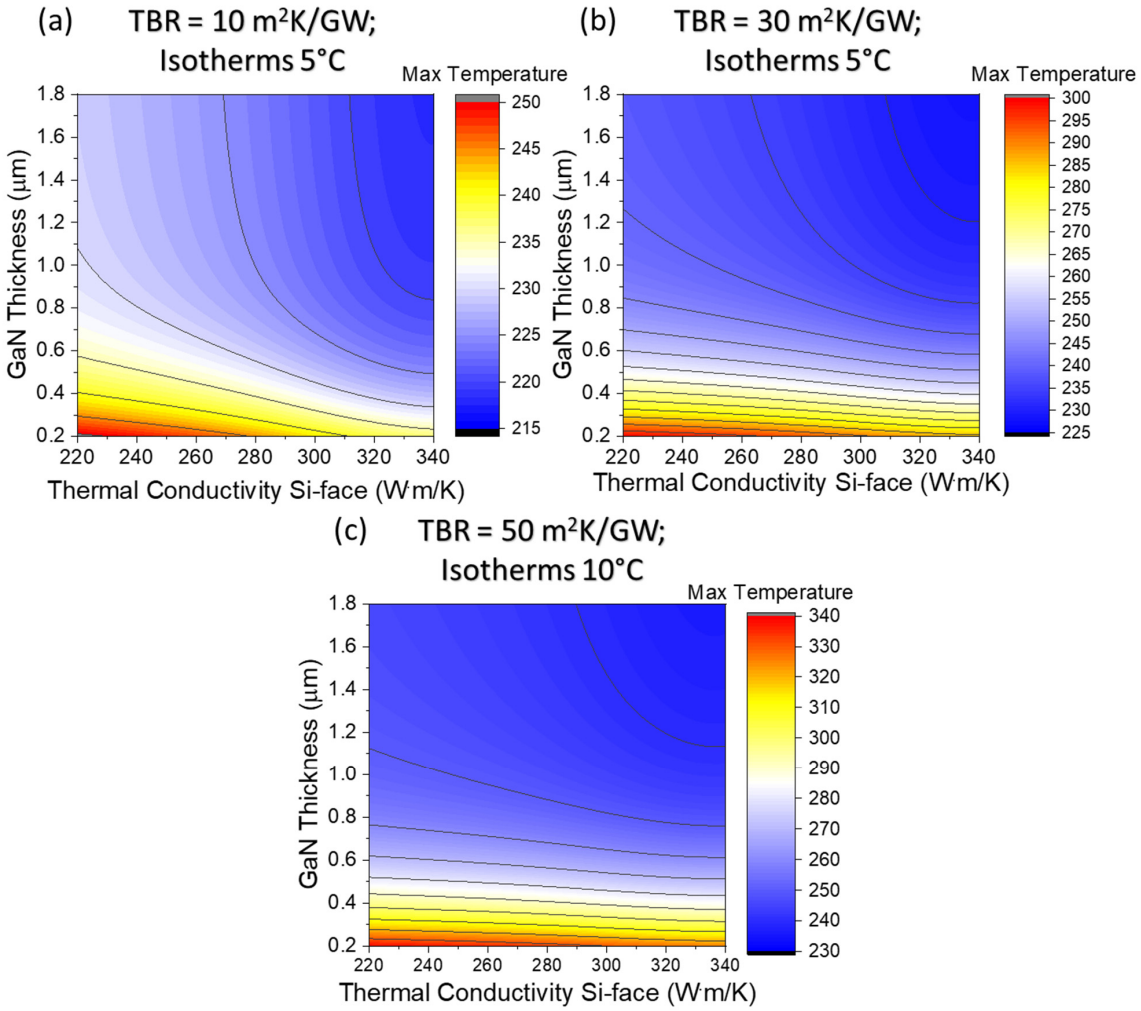

Fig. 4. Parameter space plots investigating the importance of the subsurface SiC thermal conductivity on the Si face as well as GaN thickness for three TBR_{eff} values. Simulations all undertaken with a power dissipation of 5 W mm^{-1}.

These examples are for the sample from vendor 1 and a lowering of the thermal conductivity for the Si face is evident. The results for all samples and faces investigated are given in Table 1. The largest difference was seen for the substrates from vendor 1 and 3. Both these samples showed a higher thermal conductivity for the more roughly polished C face. It is likely that the increased processing involved in reducing the surface roughness of the Si face is resulting in significant subsurface damage, reducing the phonon mean free path on average in the first ~25 µm of the SiC (the penetration depth of the TTR). These two samples possessed the highest measured thermal conductivities (300 and 343 W m^{-1} K^{-1}) suggesting that this affect is mostly observed in substrates with a high initial crystal quality. For samples with poorer crystal quality, it is likely the high number of pre-existing defects means the effect of polishing is negligible.

In Fig. 3 the role of the near surface SiC thermal conductivity on device temperature of a GaN-on-SiC ten-finger RF transistor is examined. In this simulation the measured C-face thermal conductivity was taken as the bulk thermal conductivity from either vendor 1 or 3. These results suggest that the thermal conductivity of the subsurface SiC could play a significant role in thermal management of a device. In the worst case (vendor 3), the drop off in thermal conductivity could result in a peak channel temperature rise of 10°C. These simulations underline that, with the increase in readily available, good crystal quality SiC, understanding how different polishing techniques can cause an increase in phonon scattering centres is important for optimal thermal management.

Further simulations were carried out to investigate the importance of the subsurface SiC thermal conductivity in relation to other parameters such as TBR_{eff} and GaN thickness, keeping the bulk SiC thermal conductivity fixed at the values provided by Wolfspeed (cross-plane 390 and in-plane 490 W m^{-1} K^{-1}) [9] (Fig. 4). The importance of GaN thickness is shown for three TBR_{eff} values ranging from the state of the art (10 m^2 K GW^{-1}) to a highly thermally resistive interface (50 m^2 K GW^{-}

[1]). This is an interesting parameter space to explore given the recent interest in buffer-free GaN-on-SiC devices which have shown excellent electrical properties [10]. In all cases, the peak temperature of the device becomes more sensitive to the subsurface SiC thermal conductivity with thinner GaN. It is important to recall that thin GaN layers have a much-reduced thermal conductivity compared to thicker layers. Ziade *et al*. showed that for layers <400 nm, the thermal conductivity dropped well below 100 W m^{-1} K^{-1} [5]. Somewhat counter intuitively, reducing the thickness of the GaN buffer could result in an increased thermal resistance between the device hot spot and the heat sink. Additionally, a thinner GaN buffer results in higher local heat fluxes at the interface due to less lateral heat dissipation. Hence, the heat spreading of the near surface SiC becomes increasingly more important in reducing peak temperatures. For all $TBR_{eff=}$ values, the subsurface SiC thermal conductivity has a similar effect although there is a greater temperature range for higher TBR_{eff} values. In reality TBR_{eff} is the most important factor to be considered in the thermal management of these devices. However, for interfaces with very low thermal resistance and thin GaN layers, it may become and important parameter to consider when estimating peak temperatures of devices and trying to optimise thermal management. Whilst the lowering of subsurface thermal conductivity of SiC has not been observed previously, much work has been carried out on devices with thick buffer layers. In this circumstance, the effect of the lowered thermal conductivity becomes very small and could be easily accounted for by variation of other parameters.

IV. CONCLUSION

We have shown that the thermal conductivity of 4H-SiC can vary significantly from Si face to C face of the same wafer dependent on the polishing technique employed. For the best quality SiC substrates, CMP appears to increase the number of phonon scattering centres in the first few tens of microns of the SiC, reducing its thermal conductivity. The importance of this region in the thermal management of GaN-on-SiC RF transistors has been demonstrated using FEA simulations; the lowering measured in this work could result in an increased peak temperature of 10°C for the worst-case scenario of the substrates studied. This parameter could become increasingly important for buffer-free GaN-on-SiC transistors.

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