A PNP-GaN Gate AlGaN/GaN HEMT with Improved Gate Characteristics

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Abstract

The PNP-GaN gate AlGaN/GaN high electron mobility transistor was proposed and demonstrated in this study by adding a PN-GaN diode into the p-GaN gate structure to form a PNP-GaN gate structure. The new gate structure blocks the hole injection and improves the gate reliability verified by TCAD simulations. The new PNP-GaN gate structure can reduce the electric field on the Schottky diode and redistribute the maximum electric field from the metal Schottky gate to the NP-GaN diode due to additional voltage drops. Compared to the p-GaN gate structure, the PNP-GaN gate structure exhibits a lower gate leakage current (~ 3.4 × 10^{-3} mA/mm @ V_{GS} =10 V) and a higher gate breakdown voltage 19.8 V. Moreover, the PNP-GaN gate HEMT shows a large threshold voltage (V_{TH}) of 2.96 V, a high on/off current ratio of 9.4 × 10^{8}.

INTRODUCTION

GaN-based high electron mobility transistors have shown attractive prospects in high power switching applications due to GaN excellent material properties [1–3]. The presence of 2DEG in the AlGaN/GaN heterostructure makes the device operate in a normally-on mode [4]. Normally-off operation devices are preferred in power switching applications to provide failsafe requirements and simplify gate driver design [5]. Therefore, several normally-off GaN HEMTs techniques have been proposed, such as recessed gate [6–7], fluorine ion implantation [8–9], p-type (Al)GaN gate [10–11], and cascode configuration. The p-GaN gate is currently a common choice for commercialization in these structures. The p-GaN gate HEMTs can generally be classified into two types based on the gate structures. One is the Schottky contact between the gate metal and p-GaN, another is the ohmic contact between the gate metal and p-GaN. However, the Schottky type p-GaN gate HEMT show lower gate leakage compared to ohmic type p-GaN gate HEMT due to reverse Schottky diode under the forward gate bias [12–13]. But the operating gate bias allowed for long-term operation is only 6 V. The gate's high leakage current and breakdown under higher gate bias limit the gate voltage swing. Moreover, p-GaN gate HEMTs have low threshold voltage (V_{TH}). The lower V_{TH} makes it impossible to prevent the false turn-on of the transistors caused by pulse, electromagnetic interference, noise, and high slew rate disturbance in the switching power circuit application [14]. Thus, p-GaN gate HEMTs need to effectively suppress gate leakage current and enlarge forward gate breakdown voltage [15–16]. A large positive V_{TH} also be required to prevent false turn-on in power switching applications. Many approaches have been proposed to solve these issues. For instance, the MIS gate structure is an improved way. The addition of the insulator layer can effectively reduce the gate leakage current and improve gate voltage swing. The insulator's voltage drop can also increase V_{TH} [17]. The conventional p-GaN gate HEMT with Schottky gate contact can be modeled as two back-to-back diodes at the gate region (Fig. 1(a)) [18]. One is metal/p-GaN Schottky junction (D1), another is p-GaN/AlGaN/GaN heterojunction (D2). It is necessary to redesign these two diodes to increase the threshold and input gate voltage ranges. C. Wang et al. had proposed a PNJ HEMTs which uses the NP-GaN diode to replace the original Schottky gate junction. The additional voltage drop (depletion region) on the n-GaN ensures the device withstands higher gate voltage. [19]

This work proposes a new type of gate structure (PNP-GaN gate HEMT) to improve the gate leakage current and V_{TH}. The PNP-GaN gate HEMT with Schottky gate contact can be modeled as two pairs of back-to-back diodes at the gate region (Fig. 1(b)). When the gate is under the forward biased, some voltage drops are on the PN-GaN diode (D3) and the NP-GaN diode (D4), resulting in a higher gate bias required to turn on the transistor; thus, V_{TH} is increased. Moreover, the additional NP-GaN diode produces a barrier under the forward gate bias so that the leakage current of the gate can be suppressed. The gate breakdown is improved because the maximum E-field shifts from the D1 Schottky junction to the NP-GaN diode D4.

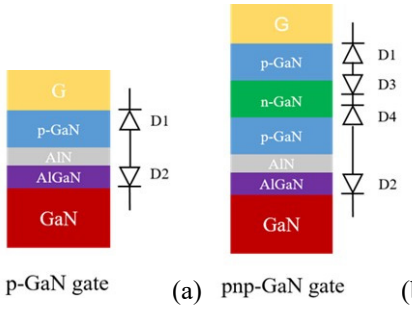

Fig. 1. Equivalent diodes of (a) p-GaN gate and (b) PNP-GaN gate structures.

DEVICE STRUCTURE AND FABRICATION

Fig. 2(a) shows the schematic cross-section of the proposed PNP-GaN gate AlGaN/GaN HEMT. The epitaxial layers were grown by MOCVD on a 6-inch Si substrate. The PNP-GaN gate AlGaN/GaN HEMT structure comprises a buffer layer, a GaN channel layer, a 15 nm $Al_{0.25}GaN_{0.75}N$ barrier layer, and a 1 nm etching stop layer. The PNP-GaN gate stack consists of two 80 nm p-GaN layers and one 80 nm n-GaN layer. Fig. 2(b) shows the secondary ion mass spectroscopy (SIMS) depth profiles of the PNP-GaN gate HEMT epitaxy before device fabrication. This study uses the depth profiles in the SIMS to confirm the p-GaN/n-GaN/p-GaN doping situation in the epitaxy. The Mg doping concentration of top p-GaN is approximately 5×10^{19} cm^{-3}, and the lower p-GaN is about 3×10^{19} cm^{-3}. The Si doping concentration of n-GaN is around 3×10^{19} cm^{-3}. Fig. 2(b) also suggests that the Mg atoms diffused into the AlGaN barrier and GaN channel, which will reduce the carrier density of 2DEG [20].

The device fabrication started with an inductively coupled plasma (ICP) dry etching to remove the PNP-GaN stack outside the gate region. After the etching process, the p-GaN was activated by rapid thermal annealing (RTA) at 800°C for 300 s in a nitrogen atmosphere. The device isolation was performed using argon ion implantation. The source/drain metals with Ti/Al/Ni/Au were deposited by electron beam evaporation and annealed at 850°C in a nitrogen atmosphere by RTA. The gate metals with Ni/Ti/Al/Ti/Au were deposited by electron beam evaporation and followed by SiN passivation layer. Finally, the pad metals with Ti/Al/Ti/Au were deposited after opening the SiN windows by reactive ion etching (RIE). The fabricated device has a gate width (W_G) of 50 µm, a PNP-GaN length ($L_{PNP\text{-}GaN}$) of 4 µm, a gate length (L_G) of 2 µm, a gate-source distance (L_{GS}) of 3 µm, and a gate-drain distance (L_{GD}) of 7 µm.

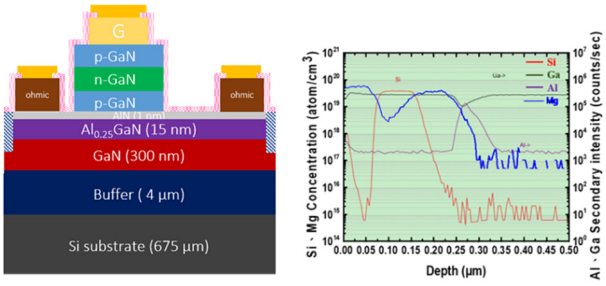

Fig. 2. (a) Schematic cross-section of the PNP-GaN gate HEMT and (b) SIMS depth profile of the PNP-GaN gate HEMT epitaxy.

RESULTS AND DISCUSSION

The band diagram and electric field (E-field) distribution at V_{GS} = 6V of the PNP-GaN gate HEMT were simulated by Silvaco TCAD, as shown in Fig. 3. The physical mechanism of additional PN-GaN diodes (D3 and D4) could be explained by the band diagrams in Fig. 3(a) and (b). In the PNP-GaN gate structure, the PN-GaN diode (D3) on the upper layer shows an effective thicker barrier to the holes in the gate metal under the forward gate bias due to the additional n-GaN existence. When a forward bias is applied to the gate, the NP-GaN diode (D4) is reverse bias. A depletion region is formed in the NP-GaN diode (D4) and supports most gate bias. The p-GaN gate HEMT can't be allowed for long-term operation under high gate voltage due to the gate leakage current caused by the high electric field in the Schottky diode (D1) [21]. The electric field distributions in the gate area at V_{GS} = 6 V are shown in Fig. 3(c) for the p-GaN gate HEMT and the PNP-GaN HEMT. It is clearly observed that the maximum E-field is shifted from the D1 junction in the p-GaN gate HEMT to the D4 junction in the PNP-GaN gate HEMT. The D4 diode is formed by the NP-GaN diode, which is much more robust than the D1 Schottky junction under the reverse bias. Moreover, the new gate structure shows a lower E-field at the D1 junction. The lower E-field at the Schottky diode in the PNP-GaN gate HEMT increases the gate reliability and bias range. Based on these results, the new PNP-GaN gate structure can suppress gate leakage current and increase gate driving range. The improved gate reliability is expectable.

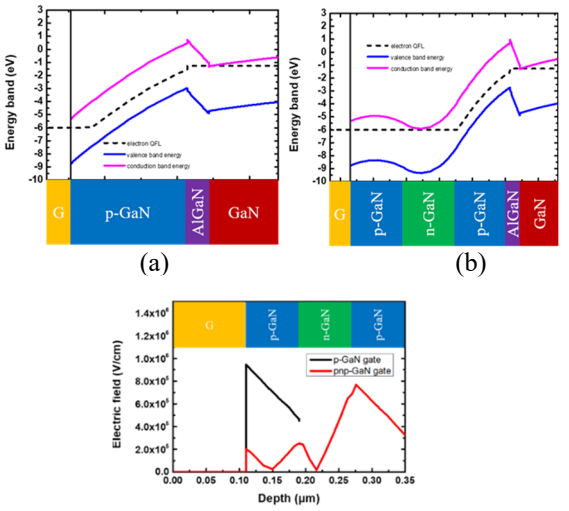

Fig. 3. The band diagrams of (**a**) p-GaN gate HEMT and (**b**) PNP-GaN gate HEMT. The electric field distribution in the gate region of p-GaN gate HEMT and PNP-GaN gate HEMT. (V_{GS} = 6V)

Fig. 4(a) shows the I_D-V_{GS} and transconductance (Gm) of the PNP-GaN gate HEMT. The proposed device demonstrates a large V_{TH} of 2.96 V defined at I_D = 1 mA/mm, a subthreshold swing of 164.1 mV/dec, and minor hysteresis. The high I_{ON}/I_{OFF} ratio of the device is close to 10^9. Fig. 4(b) shows the output current of 187 mA/mm and the on-resistance (R_{ON}) of 16.1 Ω·mm.

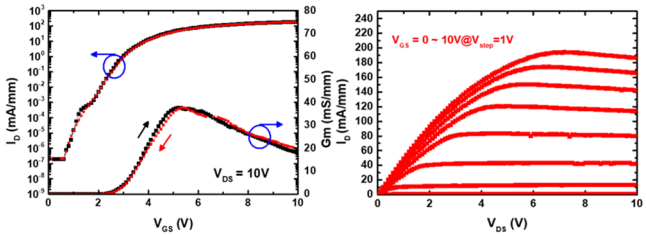

Fig. 4. (a) Measured I_D-V_{GS} and Gm, and (b) output characteristics of the PNP-GaN gate HEMT.

To observe the effect of additional PN-GaN layers, the proposed PNP-GaN gate HEMT is compared with the traditional p-GaN gate HEMT. Fig. 5 (a) shows the transfer characteristics of the PNP-GaN gate HEMT and p-GaN gate HEMT. The PNP-GaN gate device requires more gate bias to turn on, so the V_{TH} is increased but accompanied by the subthreshold swing. The gate leakage current of p-GaN gate HEMT at V_{GS} = 10 V and V_{DS} = 10 V is 147 times higher than the PNP-GaN gate HEMT. Compared with the traditional p-GaN gate device, the new gate structure exhibits a larger V_{TH} and low gate leakage current. Fig. 5(b) shows the ratio of drain current (I_D) divided by gate leakage current (I_G). The main observation is the I_D/I_G ratio decrease after devices turn on. The I_D/IG ratio of the p-GaN gate HEMT decreases rapidly after the device is turned on, while the new PNP-GaN gate HEMT falls slowly and still has a ratio of 10^5 when V_{GS} = 10 V.

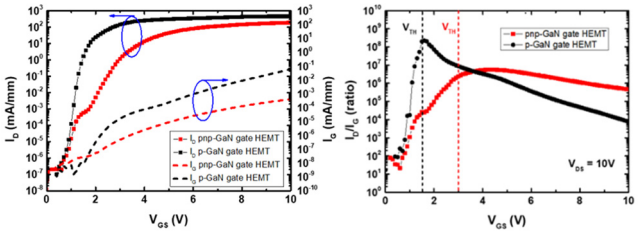

Fig. 5. (a) I_D-V_{GS} and I_G-V_{GS} characteristics, and (b) I_D/I_G ratio of the PNP-GaN gate HEMT and p-GaN gate HEMT at V_{DS} =10 V

Fig. 6(a) shows a smaller gate leakage of the new PNP-GaN gate HEMT than the p-GaN gate HEMT, and the forward gate breakdown voltage was improved from 12.5 V to 19.8 V. Compared with p-GaN gate HEMT, a larger gate driving range is allowed for PNP-GaN gate HEMT. Fig. 6(b) shows the benchmark compared to other research [19], [22–26]. The devices in [22–25] are traditional p-GaN gate structures. The gate breakdown voltage of the traditional p-GaN gate structure is lower. Devices in [19] and [26] are new gate structures proposed recently. The PNP-GaN gate HEMT shows a similar gate breakdown voltage and gate leakage current in [19] and [26] but a higher V_{TH}.

The gate reliability was performed by the time-dependent gate breakdown (TDGB) to evaluate the new PNP-GaN gate structure. The constant bias conditions are V_{DS} = 0 V and three V_{GS} biases (15, 15.5, and 16 V). At least three devices are measured at each bias point. The time to breakdown is defined as when gate leakage shows a sudden increase and gate leakage current reaches 10 mA/mm. As shown in Fig. 7(a), it can be observed that the higher the gate bias voltage, the shorter time to break down. Bringing the results into the Weibull distribution can estimate the ten-year life of the device. A linear fitting line was used to estimate the TDGB of the PNP-GaN gate HEMT (Fig. 7(b)). By calculating a lifetime of 10 years for a 63% failure level, the estimated maximum V_{GS} of PNP-GaN gate HEMT is 10.5 V which is higher than the traditional p-GaN gate HEMTs [23–25], [27–28].

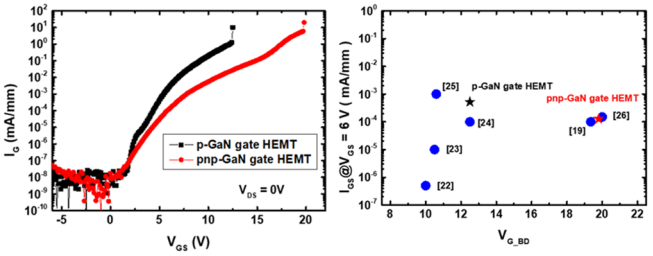

Fig. 6. (a) Forward gate breakdown characteristics of the PNP-GaN gate HEMT and p-GaN gate HEMT. (b) Comparison with other researches of the gate breakdown voltage and gate leakage current.

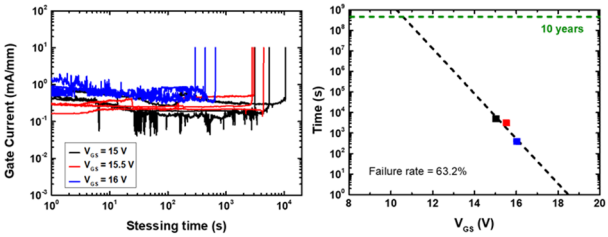

Fig. 7. (a) Gate leakage characteristics of PNP-GaN gate HEMT for TDGB measurement. (b) Lifetime prediction of the PNP-GaN gate HEMTs.

CONCLUSIONS

A new gate structure of the PNP-GaN gate in AlGaN/GaN HEMT was demonstrated in this work. The PNP-GaN stack can relocate the maximum electric field from the Schottky diode (D1) to the NP diode (D4) and thus improve the gate reliability. In addition, the extra voltage drops are on the PN and NP diodes (D3 and D4) and result in a higher turn-on voltage. Therefore, the PNP-GaN gate HEMT exhibits a high V_{TH} of 2.96 V and a low gate leakage current. The gate forward breakdown voltage was improved to 19.8 V due to a lower electric field at the Schottky diode. Thus the gate driving range is improved. The estimated maximum V_{GS} of PNP-GaN gate HEMT is 10.5 V for 10 years' lifetime at 63.2% failure level. Compared to traditional p-GaN gate HEMT, gate reliability of PNP-GaN gate HEMT is significantly improved. These results show that PNP-GaN gate HEMT can have a great potential of being used in the application of power switching circuits.

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