Overcoming Challenges in Advanced InP HEMT Manufacturing

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Abstract

Since the close of the DARPA Terahertz Electronics program, Northrop Grumman (NG) has focused on transitioning processes to 100 mm and qualifying the Advanced InP HEMT technologies for high-reliability Class A space applications. NG's 100 nm InP HEMT node is currently at a Manufacturing Readiness Level (MRL) 9 compared to the Indium Arsenide Composite Channel (IACC) nodes which are at MRL 3/4. To increase the MRL for IACC, NG has focused on transferring the processes to the 100 mm production line from material growth to wafer processing and leveraging manufacturing and qualification expertise from the 100 nm InP HEMT process. Throughout the process transfer and maturation, NG has overcome challenges with process reproducibility, yield, and throughput as well as performed extensive reliability testing.

Introduction

Over the past two decades, with funding from DARPA, NASA/JPL, and the Tri-Services, Northrop Grumman (NG) has demonstrated up to terahertz high electron mobility transistors (HEMTs) [1,2] and monolithic microwave integrated circuits (MMICs) [3-6] through aggressive scaling of the InP HEMT and the use of ultra-high mobility Indium Arsenide Composite Channel (IACC) HEMT structure, as shown in Table 1.

The key fabrication steps of the InP and IACC HEMTs are the molecular beam epitaxy (MBE), electron beam lithography (EBL) gate, thru-substrate vias (TSV), and scaled interconnect and passivation processes. The material growth and fabrication processes were originally developed on the 75 mm production line at NG. NG has focused technology maturation efforts on closing manufacturing gaps to increase the MRL [7] of the IACC nodes.

Process Overview

InP and IACC HEMT wafers are grown using molecular beam epitaxy on semi-insulating InP substrates. The IACC epi profile features a composite channel consisting of InAs layer cladded between two lattice matched $In_xGa_{1-x}As$ layers [2]. High-electron-mobility InAs channel is a key enabler of high-frequency low-DC power operation. The Schottky barrier layer and heavily doped cap are optimized for low-resistance non-alloyed Ti/Pt/Au–based ohmic contacts. Electron Beam Lithography (EBL) is used to define 25-70 nm Ti/Pt/Au–based T-gates [2]. Statistical gate process control relies heavily on Critical-Dimension Scanning Electron Microscopy (CD-SEM) to monitor gate resist opening prior to gate metallization. Timed citric acid etch with periodic current monitoring is used to etch the gate recess [2].

TABLE I
NORTHROP GRUMMAN INP HEMT
TECHNOLOGY NODE COMPARISON

Parameter / Feature	Technology Node			
	InP HEMT	IACC70	IACC35	IACC25
Gate Length (nm)	100	70	35	25
Operational Frequency (GHz)	<120	<200	<300	<1000
$In_xGa_{1-x}As$ Channel In (%)	60	100	100	100
R_c (mΩ.mm)	120	40	40	40
g_{mp}@1V (mS/mm)	1400	2200	2500	3000
Source-Drain Spacing (μm)	2	1.5	1.5	1.0
Wafer Size (mm)	100	100	75	75
Substrate Thickness (μm)	75	75	50	25
Manufacturing Readiness Level	9	4	4	3

Production MBE Transfer

Initial material and process developments were done using 75 mm wafers. Electron mobilities in excess of 15,000 cm^2/Vs have been demonstrated on 75 mm IACC HEMT material proving its high quality. To reduce epi growth and wafer fabrication cost, the growth has been transferred from single-wafer MBE tools to a multi-wafer 100 mm MBE platform. One of the key challenges was optimizing the low-temperature channel growth for large multi-wafer heaters with much higher thermal inertia in comparison to single-wafer tools. As Figure 1(a) shows, growth optimization efforts resulted in electron mobilities in excess of 13,000 cm^2/Vs on 100 mm wafers.

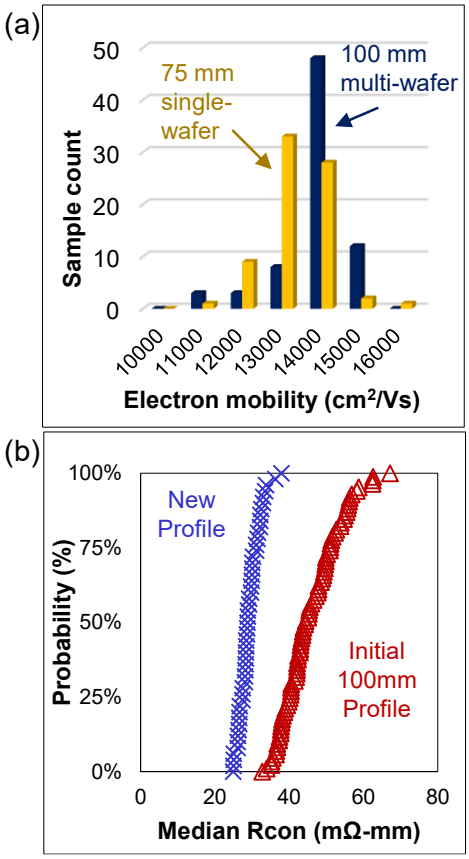

Fig. 1. (a) IACC HEMT channel electron mobilities measured on calibration wafers grown on 75 mm single-wafer and 100 mm multi-wafer MBE tools; (b) Ohmic contact resistance (Rcon) probability distributions for initial and improved 100 mm IACC profiles.

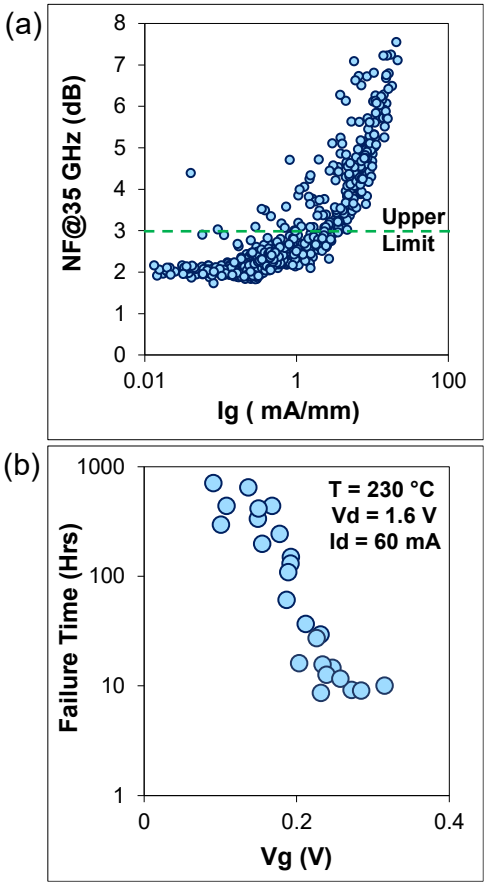

Fig. 2. Impact of non-uniform gate recess etch process on MMIC yield and reliability for IACC70: (a) 35 GHz LNA noise performance versus gate current (single wafer data); (b) Failure time versus initial gate bias used as a measure of gate recess depth.

Additional epi profile optimization efforts on 100 mm wafers were focused on improving non-alloyed ohmic contacts. As shown in Fig. 1(b), early 100 mm IACC HEMT showed large variation in ohmic contact resistance (Rcon). The doped cap design was later modified to reduce the median contact resistance down to 30 mΩ-mm and significantly minimize its variability.

IACC Gate Process

Gate formation is the most critical device fabrication step and must be carefully tuned to consistently achieve uniform electrical characteristics and high gate yield across the 100 mm wafers. A key challenge for high yield on 100 mm wafers is gate recess etch uniformity. Gate recess depth defines many key device parameters such as device transconductance, pinch-off voltage, and device breakdown. As shown on Fig. 2(a), poor control over gate recess depth can lead to Enhancement-mode (E-mode) devices with extremely thin Schottky barriers, very high gate leakage, and poor noise performance. Furthermore, E-mode devices with high gate leakage also tend to have worse reliability. Fig. 2(b) shows an example of failure time distribution for parts from one wafer with highly variable gate recess depth. The large variation in gate bias corresponding to a specific drain current reflects the large variation in gate recess depth across the wafer. Parts with more positive gate bias values corresponding to smaller gate-to-channel separation tend to have much shorter failure times for metal-diffusion driven failure mechanism.

NG has demonstrated gate recess uniformity improvements through two approaches. Fig. 3(a) shows the transfer curves from an InP HEMT wafer with a very non-uniform gate recess etch. The first approach relies on optimizing wet etch processes and semiconductor surface treatments to achieve uniform etch initiation and progression across 100 mm wafers (Fig. 3(b)). The second approach to solving gate recess etch uniformity requires the use of an etch-stop process where the wet etch selectively stops on a layer embedded into the barrier as shown in Fig. 3(c). While demonstrating excellent uniformity, this approach often requires some trade-off with device performance. To increase the process margin, in many cases these etch-stop processes

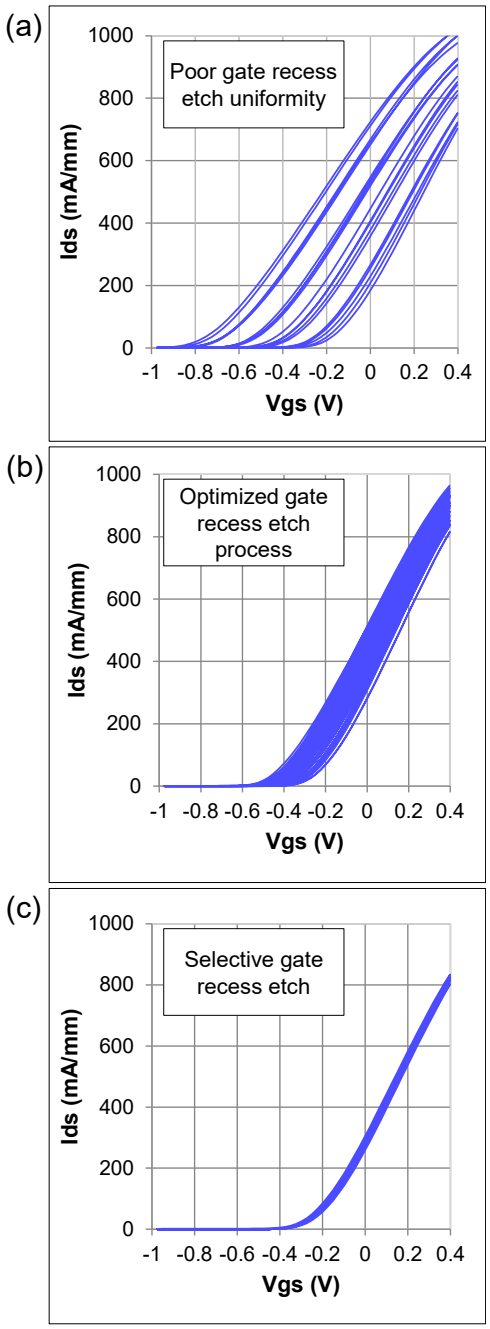

Fig. 3. 100 nm InP HEMT performance variation within single 100 mm wafer for (a) highly non-uniform gate recess etch process; (b) optimized wet recess etch process; (c) selective gate recess etch process with etch stop layer.

have a significant amount of over-etch built-in which results in undesired recess region widening and access resistance increase which in turn leads to lower device gain.

RELIABILITY

NG performs extensive life testing to demonstrate device reliability for all InP HEMT technology nodes in the initial qualification of the technology for space applications. All manufacturing improvements on qualified technologies are subjected to additional reliability testing if the changes may impact reliability. Fig. 4(a) shows 2-temperature accelerated life-test data for 100 mm InP HEMTs fabricated using selective gate recess etch process. Fig. 4(b) shows the projected median time to failure (MTTF) of 1.9×10^7 hours at transistor junction temperature of 125 °C demonstrating high reliability for Class A space missions.

CONCLUSIONS

Northrop Grumman's Advanced InP HEMT technology nodes present unique manufacturing challenges due to the highly scaled material and wafer fabrication processes. NG developed several approaches to successfully overcome these challenges on the 100 nm InP HEMT and the IACC nodes. The remaining IACC manufacturing gaps in yield and uniformity are the key focus points for the NG technology maturation efforts going-forward.

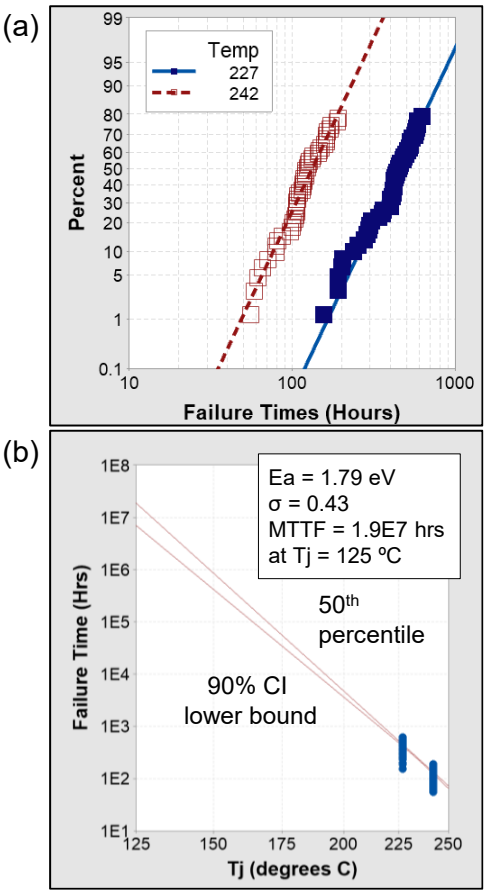

Fig. 4. 2-temperature accelerated life test results for InP HEMT process with selective gate recess process: (a) Failure time probability plot; (b) Relation plot (fitted Arrhenius).

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ACRONYMS

CD-SEM: Critical Dimension Scanning Electron Microscopy
DARPA: Defense Advanced Research Projects Agency
EBL: Electron Beam Lithography
HEMT: High Electron Mobility Transistor
IACC: Indium Arsenide Composite Channel
InP: Indium Phosphide
MBE: Molecular Beam Epitaxy
MMIC: Monolithic Microwave Integrated Circuit
NG: Northrop Grumman
TSV: Thru-Substrate Via