Manufacturing Challenges of Czochralski Growth and Fabrication of 2-inch Semi-Insulating β-Ga_2O_3 Substrates

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Keywords: gallium oxide, Czochralski, crystal growth, CMP, semiconductors

ABSTRACT

In recent years, beta-phase gallium oxide (β-Ga_2O_3) has emerged as an attractive candidate for next generation high voltage power switching and high frequency transistors. This is primarily due to its ultra-wide bandgap of 4.9 eV and high electric field breakdown of 8 MV/cm as well as being the only wide bandgap semiconductor capable of crystallization from a melt utilizing industrial scale manufacturing techniques such as the Czochralski (CZ) method. CZ crystal growth, fabrication, and polishing of β-Ga_2O_3 single crystals introduce unique process challenges not encountered with other compound semiconductors. Fabrication of single crystal β-Ga_2O_3 boules into epi-ready substrates is complicated by the presence of active (100) and (001) cleavage planes which are highly susceptible to mechanical stress and can easily form cracks during boule fabrication processes such as coring, outside diameter and flat grinding, wire sawing, and polishing. In this paper, we will review an Air Force Research Laboratory (AFRL) funded effort with SYNOPTICS and the Penn State University Applied Research Laboratory (PSU/ARL) for development and commercialization of 2-inch semi-insulating (010) β-Ga_2O_3 substrates with improved crystalline quality and sub-nm surface roughness. In this effort, improvements were made in boule growth and processing into wafers, the depth of damage for wafer processing steps was analyzed and shown to be up to 100 µm, and an improved, high removal rate, multi-step polishing process was developed to eliminate subsurface damage. This process yields in an epi-ready surface with a ~10X reduction in polishing cycle time. Typical x-ray rocking curve measurements for the new process were consistently < 75 arcsec with an average surface roughness of < 3 Å. Additionally, an etching and mapping method was developed to analyze dislocation and nano-pipe distribution and map defect density for 2-inch wafers.

INTRODUCTION

In recent years, β-Ga_2O_3 has emerged as an attractive candidate for next generation high voltage switches for both RF power amplification and power switching electronics. This is primarily due to its ultra wide bandgap of 4.9 eV and very high electric field breakdown of 8 MV/cm. This translates into a Baliga Figure of Merit (BFOM) estimated to be several times higher than that of SiC or GaN. The critical field strength is also a key factor in Johnson's Figure of Merit (saturation velocity-critical electric field product, $v_{sat} \cdot E_c$) used to describe RF operation. [1] Additionally, β-Ga_2O_3 is the only wide bandgap semiconductor capable of crystallization from a melt utilizing industrial scale manufacturing techniques. The application of melt-based growth techniques provides significant manufacturing, cost, and scalability advantages compared to vapor transport processes used for other wide bandgap single crystals such as SiC, GaN and AlN. The commercial availability of bulk β-Ga_2O_3 substrates has enabled rapid device progress since the first β-Ga_2O_3 MESFET demonstration in 2012 [2]. Record device results and the prospect for growing large diameter, low cost β-Ga_2O_3 bulk crystals for substrate wafers provides an added incentive for development and commercialization of this promising next generation semiconductor material.

EXPERIMENTAL

Overview

In early 2020, SYNOPTICS demonstrated the growth and fabrication of 2-inch Fe-doped (010) β-Ga_2O_3 boules grown by the Czochralski (CZ) method. This achievement overcame numerous challenges associated with boule fabrication and substrate polishing was shown to be reasonably reproducible. The primary challenge has been fabrication and polishing of these boules into epi-ready substrates. During the past 18 months, SYNOPTICS partnered with the Penn State University Applied Research Laboratory (PSU/ARL) to improve the manufacturability of 2-inch substrates with the goal of improving quality and reducing cycle time.

Crystal Growth

2-inch diameter Fe-doped (010) β-Ga_2O_3 boules were grown by the CZ method in 3.5-inch diameter iridium (Ir) crucibles. Doping was intentionally varied from around 0.0025 to 0.01 mol% Fe. A significant challenge related to β-Ga_2O_3 crystal growth is balancing the oxygen (O_2) partial pressure. A sufficiently O_2-rich atmosphere is required to

reduce melt decomposition/β-Ga_2O_3 dissociation. However, a high O_2 partial pressure severely oxidizes the Ir crucible. With the notable increase in the price of Ir over the past two years, this has become an even more important consideration for process scaling. For the CZ method, the mixture of carbon dioxide (CO_2)/O_2 was optimized to suppress β-Ga_2O_3 dissociation during growth while also preventing excessive oxidation of the Ir crucible. Additional major growth challenges included cracking and twinning of the boules. By optimizing the seed diameter and paying careful attention to the seed crystal alignment with respect to the [010] growth direction, cracking and twin formation in 2-inch boules were dramatically reduced. An example of a 2-inch Fe-doped (010) β-Ga_2O_3 boule grown by SYNOPTICS is shown in Fig. 1.

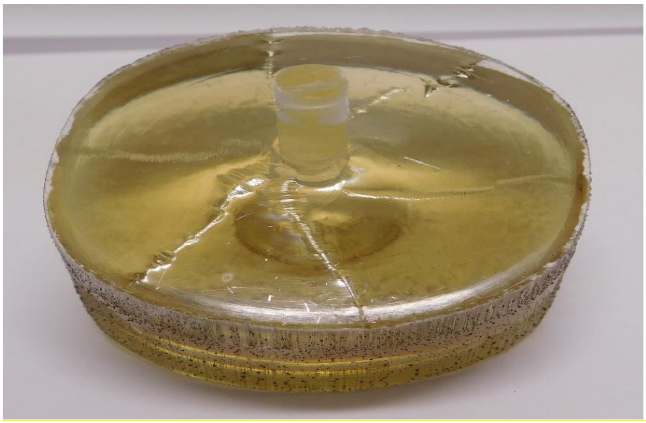


Fig. 1 Example image of a 2-inch Fe-doped (010) β-Ga_2O_3 boule grown by SYNOPTICS.

Substrate Fabrication and Polishing

Following boule growth, the ends were cropped, and the boule was ground to diameter and sliced using a Takatori multi-wire slurry saw using 9-12 µm boron carbide abrasive. This process was optimized to maximize slicing yield by rotationally clocking the boule relative to the (100) and (001) cleavage planes.

A key step in development of the polishing process was to first understand the depth of damage after slicing to ensure that virtually all damage was removed. Depth of damage was estimated based on two methods: size of the slurry saw abrasive and average surface roughness after slicing. Using both methods, the damage was estimated to be on the order of 15-20 µm. [3] To validate this estimate, cross-sections of as-wire sawn wafers were prepared and imaged by optical microscopy (OM) and scanning electron microscopy (SEM) as shown in Fig. 2. Based on these studies, we determined that the actual depth of damage in the β-Ga_2O_3 was significantly greater, ~75 µm.

To further understand and quantify subsurface damage we used in-line x-ray diffraction (XRD). Unmounted wafers were characterized, and we also developed custom polishing plates that could be mounted within a high-resolution XRD system so that x-ray rocking curves (XRRC's) could be collected at intermediate points in the process without removing wafers from the polishing plate. A series of wafers were initially analyzed at various points in the baseline polishing process as shown in Fig. 3 which plots the (020) full-width at half-maximum (FWHM) values calculated vs. total removal amount at various stages of processing, including wire sawing, grinding, intermediate polishing, and final polishing. Based on these observations, a total removal amount of ~100 µm was targeted to ensure virtually all subsurface damage was removed.

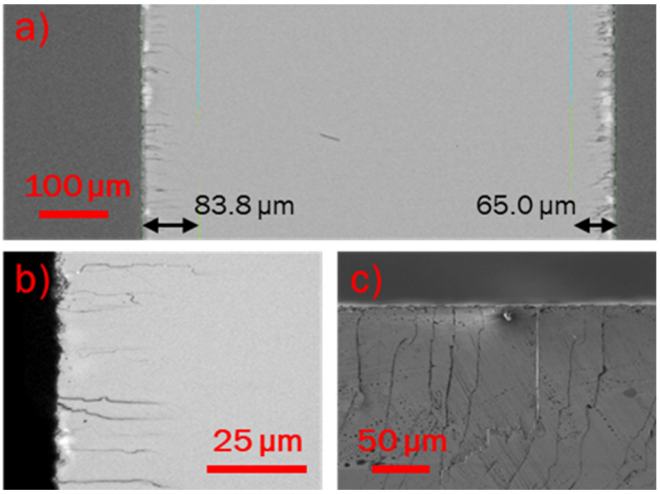


Fig. 2 Example a) OM image of a cleaved cross-section, b) expanded OM image, and c) SEM cross-sectional image showing depth of damage for a (010) β-Ga_2O_3 wafer after wire sawing.

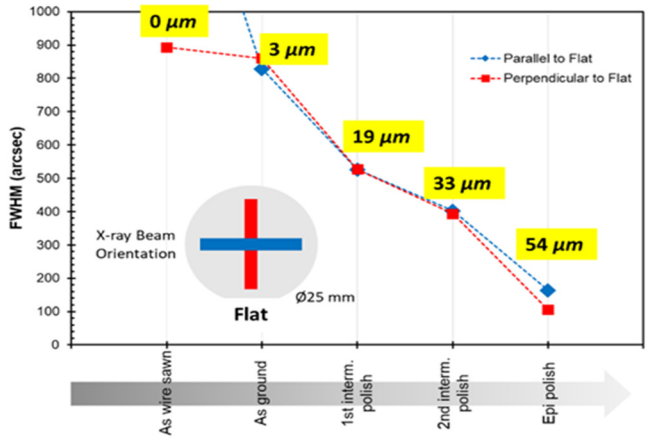


Fig. 3 (020) XRRC FWHM values calculated vs. total removal amount at various stages of processing.

The key objective in polishing development was balancing essential metrics including surface roughness, bow/warp, and defect density with cycle time and manufacturing cost. Early project results indicated that a low surface roughness (Ra < 3 Å), high quality surface could be achieved by polishing with a single step process using a colloidal silica suspension. However, removal rates were low, on the order of 0.4 µm/hr, resulting in a total polishing cycle time exceeding two weeks.

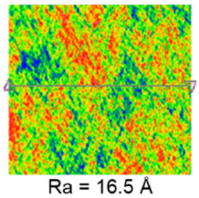
High Removal Rate Intermediate Polishing Step

To reduce cycle time, we developed a two-step polishing process with the target removal of 75 µm using an intermediate process and 25 µm during final CMP. Several options for polishing slurries, including colloidal alumina and diamond, were evaluated. Excellent results were achieved by selecting 1-3 µm diamond for the intermediate polishing step. Removal rates on the order of 25 µm/hr were obtained with this approach which reduced the polishing time for the initial 75 µm removal from ~187 hrs down to only ~3 hrs.

To characterize the surface after the diamond intermediate polishing step, we assessed substrates using XRRC's and Zygo white light interferometry (WLI). Fig. 4 shows typical results after removal of 75 µm using 1-3 µm diamond slurry. FWHM values were very low, especially considering the hardness of the polishing slurry. A consistent surface finish was also obtained, with an average surface roughness (Ra) between 15-20 Å, serving as an excellent starting point for final CMP. To validate this process, SYNOPTICS processed several sets of wafers through the final CMP step using the standard colloidal silica process. This resulted in extremely low XRRC FWHM and Ra values as shown in Fig. 4.

a) After Diamond Intermediate Polishing

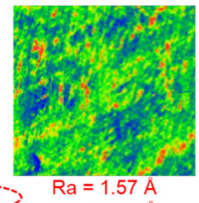
Wafer ID	(020) FWHM$_{\parallel}$	(020) FWHM$_{\perp}$
E310-261-19	87.12	72.00
E310-261-20	68.76	55.80
E310-261-21	68.04	55.08
Average	74.64	61.96



Ra = 16.5 Å
PV = 182.5 Å

b) After SYNOPTICS Final CMP

Wafer ID	(020) FWHM$_{\parallel}$	(020) FWHM$_{\perp}$
E310-261-19	39.60	35.28
E310-261-20	37.44	36.36
E310-261-21	41.04	33.12
Average	39.36	34.92



Ra = 1.57 Å
PV = 61.3 Å

Fig. 4 XRRC (020) FWHM values and Zygo WLI (0.7x0.7 mm area) scans after a) diamond intermediate polishing and b) SYNOPTICS final CMP.

Final CMP Optimization

To further optimize the process, we studied a series of alternative final CMP steps and identified two promising options. We did a study of the effect of pH modified colloidal silica over the pH range from ~3 to 9. At a pH of 4, we were able to get extremely low surface roughness values and excellent XRRC FWHM values while increasing removal rate by ~2.5X to near 1.0 µm/hr. Fig. 5 shows the results of this pH modified final CMP step for a pH of 4.0. This approach also was highly effective in removing the residual layer of slurry which tended to adhere after conventional CMP. Overall, using these two process steps we were able to reduce the total polishing cycle time for 100 µm of total removal from ~250 hrs to only ~28 hrs. Similar results were obtained using a pH modified nano-diamond slurry, providing a potential route to a non-silica based polishing process. Work is ongoing in the development of both final CMP processes.

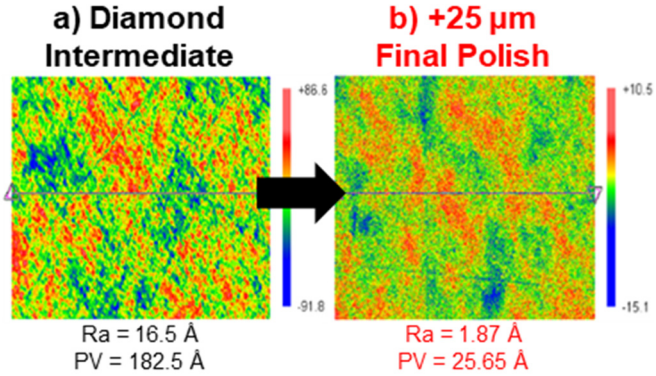


Fig. 5 Zygo WLI (0.7x0.7 mm area) scans showing surface roughness after a) high removal rate diamond intermediate polishing and b) pH modified final CMP (Z-axis scale in [Å]).

Defect Density Analysis Using Etch Pit Imaging and Mapping

To study the defect density in the (010) β-Ga_2O_3 substrates we developed an etch pitting, imaging, and mapping analysis tool. Polished wafers were chemically etched to characterize the defect density distribution. 85% phosphoric acid (H_3PO_4) was selected based on its relative β-Ga_2O_3 etch rate [4]. Full wafer maps were obtained by OM and analyzed using defect mapping software developed in-house at PSU/ARL. An example of a region of a 1-inch wafer etch pit density map and corresponding histogram are shown in Fig. 6. Etch pit densities were generally on the order of 1E+4 to 5E+4 cm^{-2}.

Individual defects were also imaged by SEM. The etch pits were classified by comparison with transmission electron microscopy (TEM) studies in the literature which assessed the three-dimensional defect structures. Type A etch pits, attributed to voids, were the most common type observed and are shown in Fig. 7a. Smaller, Type E etch pits, attributed to <010> screw-type dislocations, were also sometimes observed and are shown in Fig. 7b. [4] [5]

Work is also ongoing to prepare and image cross-sections of the etch pits observed in the (010) β-Ga_2O_3 substrates grown by the CZ method. Fig. 8 shows an example cross-sectional SEM image of a Type A defect prepared using the focused ion beam (FIB) method. This image shows the etch pit depth is slightly over 10 µm and has a three-dimensional structure resembling that observed in (010) β-Ga_2O_3 substrates grown by other methods, such as edge-defined, film-fed growth (EFG). This type of defect has also been termed a "nano-pipe" in the literature [5]. These defects are currently under additional investigation.

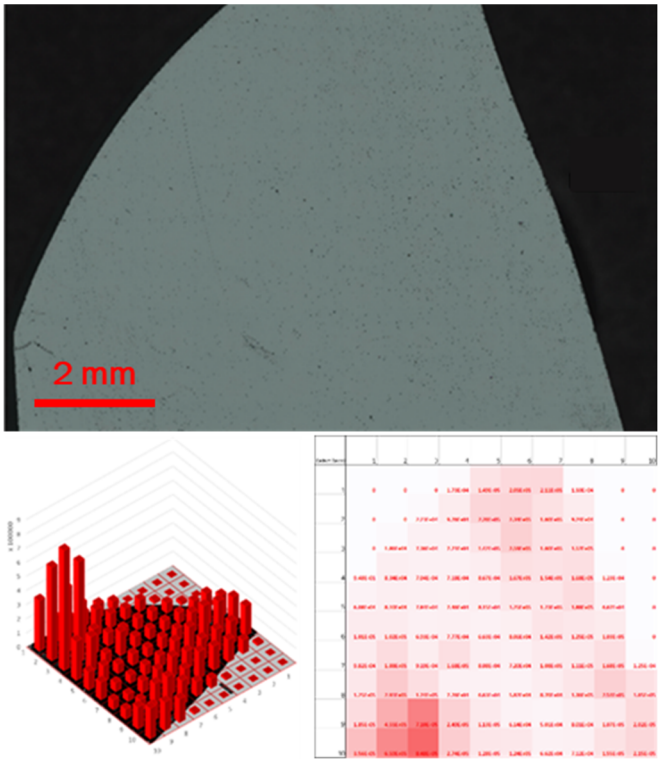


Fig. 6 Example OM image of a (010) β-Ga_2O_3 wafer after etching with corresponding etch pit density maps.

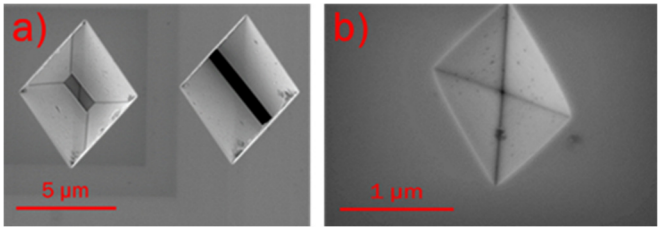


Fig. 7 Example SEM images of a) Type A etch pits attributed to voids and b) Type E etch pit attributed to a <010> screw-type dislocation.

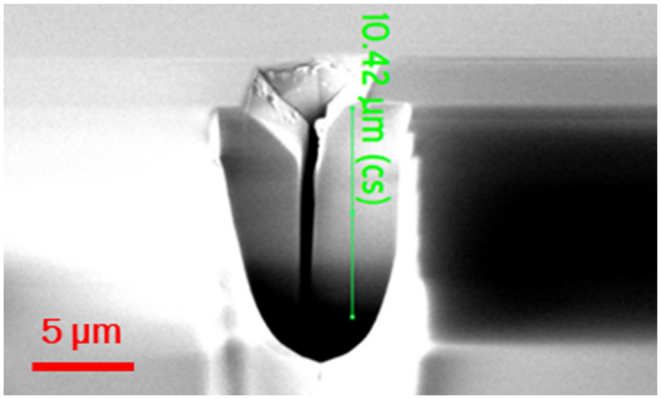


Fig. 8 Example cross-sectional SEM image of a Type A etch pit prepared by FIB showing the pit depth is > 10 µm.

CONCLUSIONS

2-inch Fe-doped (010) β-Ga_2O_3 boules were grown by the Czochralski (CZ) method and subsequently fabricated into epi-ready substrates. In this effort, progress was made addressing the CZ crystal growth challenges, including optimizing the O_2 partial pressure during growth to minimize β-Ga_2O_3 dissociation and optimizing the seed geometry to minimize cleaving. An in-line XRD method was utilized to obtain XRRC measurements as a function of total removal amount to complement surface topography data and SEM images and quantify depth of damage. A two-step polishing process was developed to efficiently remove subsurface damage while producing a surface finish necessary for epi growth and device fabrication. This process yielded a Ra < 3 Å with (020) FWHM values consistently less than 75 arcsec. The defect density distribution for the (010) β-Ga_2O_3 substrates was also investigated by etch pit analysis and full wafer mapping in which the most common types of defects were voids with a few <010> screw-type dislocations. Future work includes optimizing the pH modified final CMP process as well as a nano-diamond CMP step to avoid possible Si contamination. Overall, the fabrication/polishing process described in this paper represents a nearly 10X reduction in cycle time compared to the previous method and significant progress toward scaling up β-Ga_2O_3 substrate manufacturing.

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