Clip Bonded CCPAK-1212: Engineering the Next Generation GaN Products

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INTRODUCTION

Nexperia's commercialized GaN based power transistors show tremendous advantage in the Power device market delivering low on-resistance at 650 V. To achieve this outstanding performance for different applications (such as onboard chargers, DC-DC converters, traction inverters) [1, 2], Nexperia introduced a novel clip-bonded packaged HEMTs with low off-state leakage at high operating voltages. While being the first to introduce a fully clip-bonded solution in the GaN industry without any wire-bonded connection; This solution offers 5 times lower inductances than leaded packages (2.37 nH compared to almost 14 nH), and ultra-low package resistance including a thermal resistance of < 0.5 K/W [3]. Maintaining this performance required a high-level of device engineering from the HEMT design, the MOSFET design, and the cascode configuration in the compact CCPAK resulting in an innovative package with industry leading performance. The clip-bond configuration is for optimized thermal and electrical performance and the simplified cascode to avoid the need of gate drivers.

RESULTS AND DISCUSSION

Fig. 1 shows the wirebond free GaN HEMT and Si MOSFET in cascode configuration. These devices are sitting in an ultra-low resistance package in a compact footprint of 12x12 mm and <0.5 K/W thermal resistance. The package leads are flexible for improved reliability (from flexible connectivity, preventing clip cracking and crack propagation) and easily exposed and accessible for optical inspection. For added flexibility in designs and to further improve heat dissipation, CCPAK is engineered with both top-side cooling and traditional bottom-side cooling.

Given that the gate connection of the HEMT in this cascode configuration is at the bottom of the die to improve $R_{DS(on)}$ and eliminates floating substrate, we did need to make a connection between the gate of the HEMT and the source of the MOSFET (the usual cascode connection). In this novel package, this could be achieved externally or internally as shown in Fig. 2(a) and 2(b) respectively. If the architecture is done externally, it will require designers to perform the change on the layout of their boards, but if performed internally, this is not necessary. Thus, the design team opted for the internal version with internal pillars making this critical cascode connection. The added value of this connection is the improved thermal dissipation that is another key driver for power devices. Measurements and simulations are ongoing to give an accurate quantification of this added value. The results will be presented during the oral presentation.

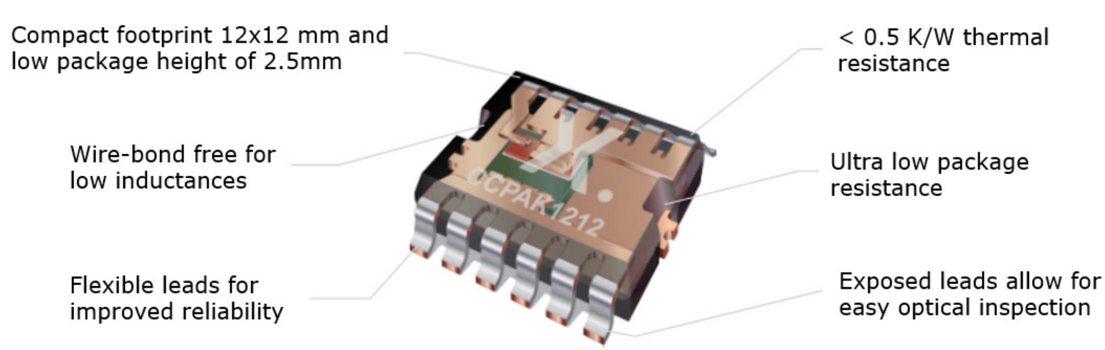

Fig. 1. Skeletal representation of the novel CCPAK Power GaN FETs. *Source: Nexperia.*

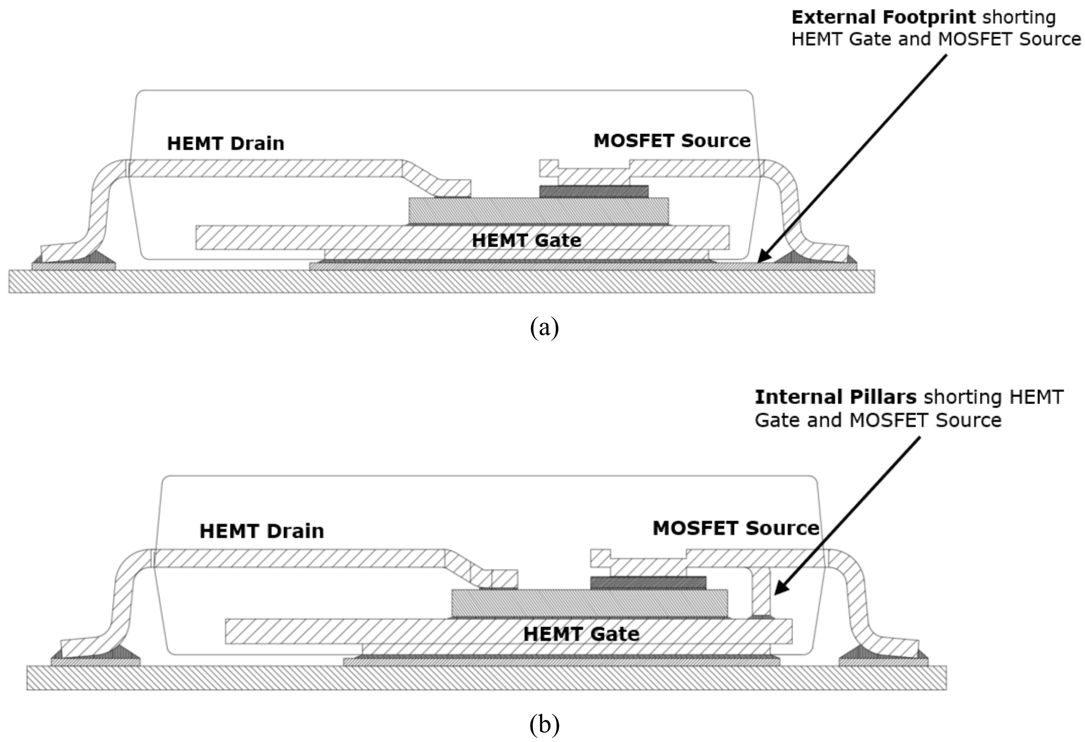

Fig. 2. – External (a) and Internal (b) connection between the gate of the HEMT and the source of the MOSFET (the usual cascode connection) in the bottom cooled devices. Nexperia is introducing option (b).
Source: Nexperia.

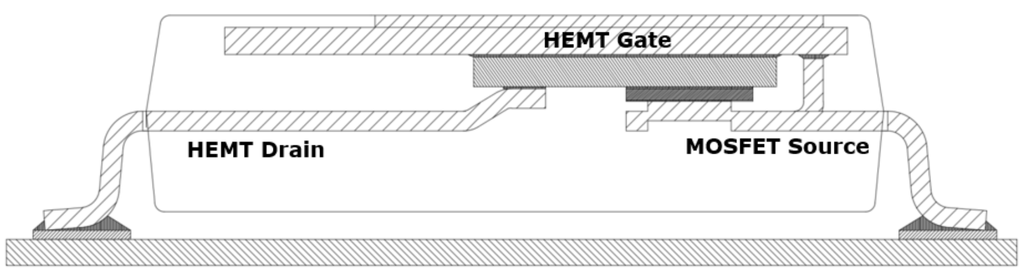

Fig. 3. Top side cooled CCPAK1212.
Source: Nexperia.

Fig. 3 shows another option where in this case the cooling is on the top side by further enhancing the chip and board heat dissipation during hard switching.

This cascode of 650V, 33 mΩ features a V_{th} of 4V with a robust gate oxide (+/- 20V). The switching time characteristics are ~10 ns for rise and fall times. To validate the robustness and high reliability of this product, 300 prototype samples were subjected to 1000h HTRB test (see Fig. 4). This is a great indicator on the robustness and high reliability of these devices addressing the field plate insulator, the buffer trapping, and the trapped charge in gate region that could consequently shift $R_{DS(on)}$ [4, 5].

Application areas (such as onboard chargers, DC-DC converters, traction inverters) are also key in making electric vehicles a real replacement for fossil-fueled internal combustion engines. Heat dissipation, power losses and power densities are among the many challenges which need to be addressed. On this journey, we also work on addressing these major challenges and data will be shown in the oral presentation. Nexperia's team is also working on circuit designs to minimize ringing due to fast switching

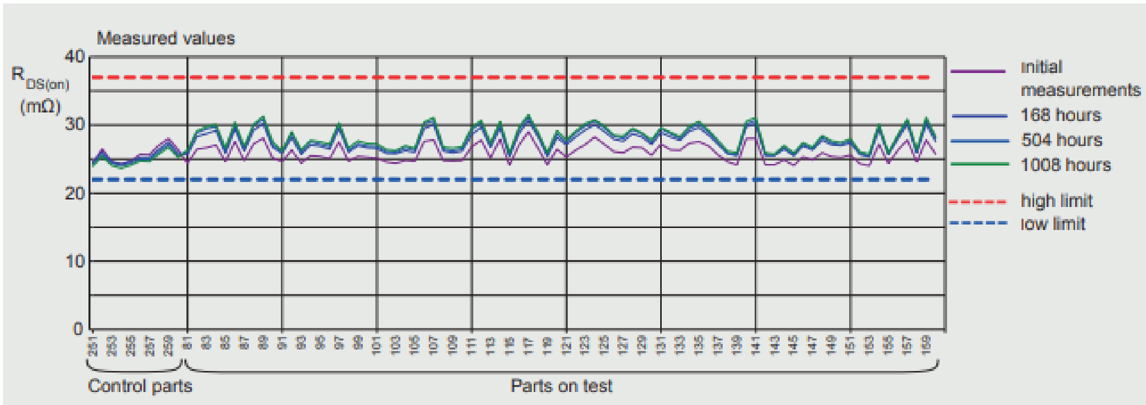

Fig. 4. Dynamic $R_{DS(on)}$ measurements during HTRB.
Source: Nexperia.

transients. Fig. 5 shows an example and a portion of PCB layout of Nexperia's half-bridge evaluation board indicating the placement of the power transistors.

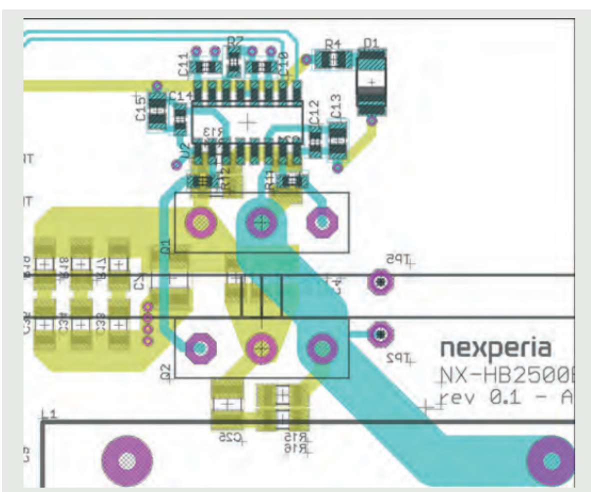

Fig. 5. Portion of a PCB layout of Nexperia's half-bridge evaluation board.
Source: Nexperia.

CONCLUSIONS

In summary, this truly innovative clip-bonded GAN039-650NBB CCPAK1212 product from Nexperia is leading the industry of commercial GaN Power Devices and application-based data will be presented showing the efficiency and power density while maintaining the performance of this commercial device.

ACKNOWLEDGEMENTS

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ACRONYMS

CCPAK: Copper Clip Package
HEMT: High Electron Mobility Transistor