Processing of Vertical GaN Power Device via Silicon Nitride Shadowed Selective Area Growth

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Abstract

It is critical to be able to develop GaN power devices with highly crystalline materials to reduce leakage currents that negatively impact performance. Silicon Nitride Shadowed, Selective Area Growth (SNS-SAG) as enabled by Plasma-Assisted Molecular Beam Epitaxy (PAMBE) is employed as a method of producing low leakage power devices. Also utilized is an edge termination scheme that is uniquely possible by the SNS-SAG method.

INTRODUCTION

In today's ever-growing power sector, the need for efficient switching devices is paramount. Additionally, these devices need to be able to support high forward currents and high reverse biases and do so over a long period of time. Gallium Nitride (GaN) is one such material that is capable of doing all of this owing to its high n-type mobility, wide band gap, and high breakdown field. GaN however, like any material, is not without its challenges. Conventional processing methods for producing GaN devices take the route of planar growth, followed by either inductively coupled plasma reactive ion etching (ICP-RIE), ion implantation, or some combination of the two. These methods have been greatly improved over the past few decades, but in GaN still result in the formation of defects which cannot be fully removed owing to the high-energy ion bombardment used which is integral to both processes. These defects serve to degrade the crystallinity of the material and result in reduction of p-type doping efficiency (which is already naturally very low in GaN), unwanted increase in n-type doping levels, and the generation of leakage pathways. Leakage pathways not only decrease the on-off ratio of the devices, but also increase the probability of avalanche breakdown which reduces breakdown voltage and increase heating which shortens the overall device lifetime [1]-[6]. In this work we present an alternative fabrication method which does not require ICP-RIE etching of GaN, nor ion implantation for doping. SNS-SAG allows us to do this by enabling growth of thick, doped layers in selective areas. As outlined in our sister paper, this method employs a bilayer SiN/SiO_2 mask which produces smooth sidewalls free of contamination and substrate-propagated defects as characterized by Cathodoluminescence (CL) Scanning Electron Microscopy (SEM), Conductive Atomic Force Microscopy (C-AFM), and X-ray Spectroscopy (XPS). Here we discuss further the applications of SNS-SAG to producing high performance devices.

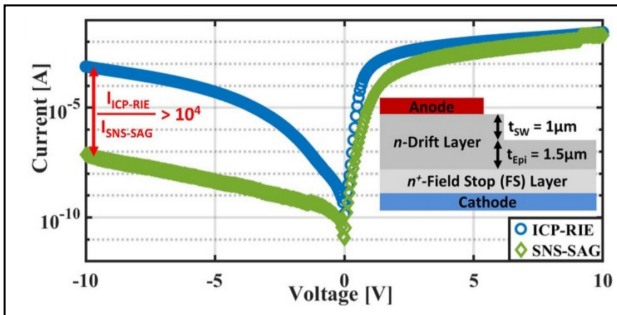

Fig. 1. Comparison of the experimental current–voltage (I–V) characteristics for devices processed using SNS-SAG and ICP-RIE. The schematic diagram of the SBD structure used to obtain I–V characteristics is shown in the inset. The portion of the drift layer indicated by thickness t_{SW} is processed using SNS-SAG and ICP-RIE.

Our preliminary work published recently shows a comparison between a device produced using SNS-SAG and one produced using a conventional ICP-RIE scheme. The devices were Schottky-barrier diodes (SBDs) consisting of a 1µm undoped mesa on top of a planar undoped layer grown on a bulk n+-substrate. The device layers were grown in parallel to provide the best possible comparison. The SNS-SAG device displayed a 10^4 reduction in leakage current, a higher turn-on voltage, and a lower specific on-resistance. The scheme and IV data are shown in figure 1. While the reason for the reduction in leakage current has already been discussed, the reasonings for the higher turn-on voltage and higher forward current are as follows. First, the damage induced in the sidewall serves to locally raise the doping level. This allows for thermionic field emission of carriers to occur more readily, creating higher current at lower voltages. However, the forward resistance is increased because this crystalline damage also serves to reduce the mobility in the sidewall [7].

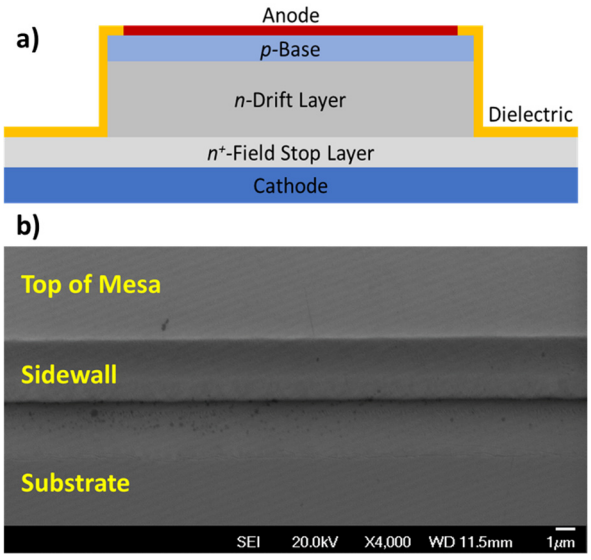

Fig. 2. a) The DiVSET p-i-n diode structure. Thicknesses are not to scale. Angle of the sidewall is not included (will not be 90°). b) An example of an SNS-SAG mesa and sidewall taken via SEM.

With this preliminary demonstration complete, we seek to extend our SNS-SAG to thicker films and more complex devices. In this work we develop a 3.5μm mesa consisting of a 3μm n-drift layer and 500nm p-type layer to form a p-i-n diode. Additionally, we employ edge termination known as dielectric vertical sidewall-appended edge termination (DiVSET). This is outlined in figure 2. The dielectric will consist of a SiN/SiO_2 bilayer which serves to both passivate the GaN surface as well as dissipate the electric field crowding in the oxide layer. The contact resistance will end up dominating $R_{on,sp}$ and will be minimized by capping the *p*-base with a thin p^{++} layer, as well as using a Ni/Au contact scheme. The DiVSET scheme also supports the inclusion of additional edge termination. A single-zone junction-termination extension can be used between the edge of the *p*-base and the dielectric sidewall. This is effective at making sure the electric field maxima spread out between the dielectric and the edge of the *p*-base [8].

Discussion

The working principle behind SNS-SAG is that PAMBE growth of GaN relies on line of sight between the material sources (primarily N) and the substrate. By restricting the line of sight and creating a "shadow", it is possible to restrict film growth in that region as shown in figure 3(a). Due to substrate rotation, shadowing is only partial, so an undercut region is used to ensure that there is no intersection between the grown mesa and the mask material as shown in figure 3(b). Such an intersection would result in a polycrystalline region being formed on the mesa. The SNS-SAG mask consists of a bilayer film of SiN_x and SiO_2. The preliminary

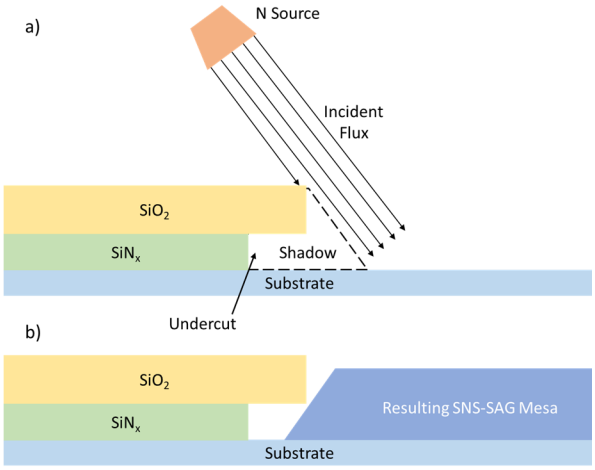

Fig. 3. a) Growth geometry that allows for SNS-SAG to occur. The shadowed region is created by restricting the nitrogen plasma flux. b) The general shape of the mesa that results from SNS-SAG. The sidewall angle can vary with the mask geometry.

1μm work consisted of using an approximately 1:2 ratio of SiN_x:SiO_2, with the total stack thickness being slightly greater than the mesa thickness. Phosphoric acid is used as a selective wet etchant to create the undercut in the SiN_x. The mask material where it is exposed to flux is coated in polycrystalline GaN that is removed during the mask removal process and is omitted from figure 3.

The most challenging aspect of extending SNS-SAG to thicker mesas is the stress engineering of the mask material. Initial attempts to do so consisted of scaling up the geometry to have a total mask thickness of 3.5μm. Doing so resulted in widespread cracking of the mask upon heating to growth temperatures (approximately 750°C) as well as some cracking of the GaN substrate along the mask features. Clearly, it is of great importance that as the substrate and mask heat from room temperature up to the growth temperature, neither the substrate nor the mask itself fracture in such a way that would degrade the electrical performance or allow for unwanted growth, respectively.

For growth studies, c-plane GaN on sapphire substrates have been used. The a-plane sapphire linear coefficient of thermal expansion (CTE) is approximately $7.9x10^{-6}$/°C which will dominate the strain of the GaN and mask layers [9]. GaN has a slightly lower a-plane CTE (between those of sapphire and the masking materials), so proper treatment of the sapphire condition will ensure improved behavior when using a bulk GaN substrate. The linear CTE of SiN_x is approximately $2.3x10^{-6}$/°C with that of SiO_2 being even lower [10]. We can therefore calculate the change in strain of the SiN_x layer to be approximately $3.92x10^{-3}$ resulting in a stress of approximately 400MPa in the SiN_x film when

going from room temperature to the growth temperature.

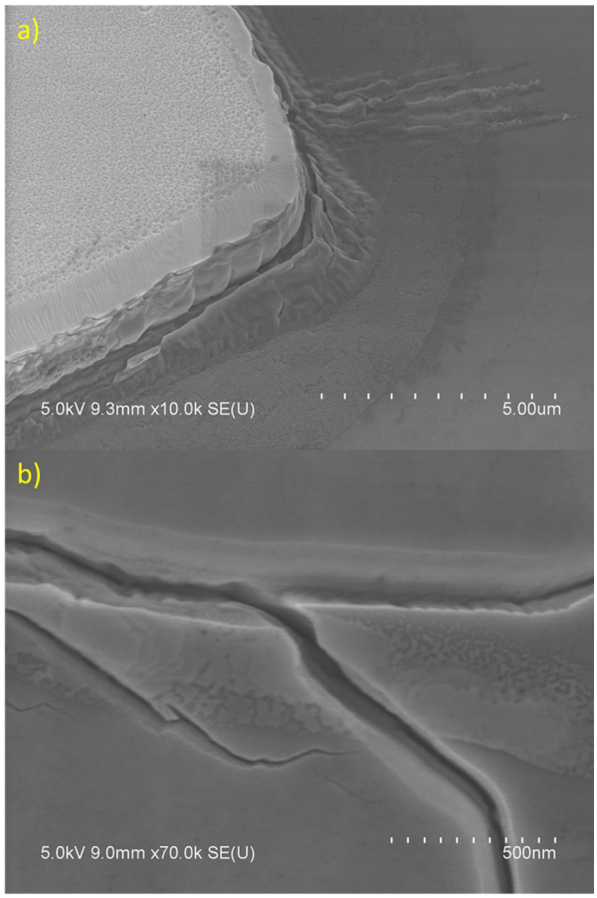

Fig. 4. a) An SEM image example of sidewall roughness and cracking caused by surface stress. Image is taken at a 30° angle with the upper left being the surface of the mesa and the right hand side being the substrate. b) An example of a crack in the surface of the GaN substrate due to surface stress.

This stress approaches reported values for fracture strength [11]-[14]. Furthermore, with the SiO_2 layer slightly restricting expansion at the top surface, stress concentrates in the lower regions of the mask. Figure 4 shows example of the damage to the GaN layers that can occur due to stress. Though not shown here, cracking and delamination of the mask can also occur leading to wide areas of undesired growth or unpredictability of the sidewall angle.

It is clear that we need to reduce the magnitude of stress in the masking material so that when it is heated it does not delaminate, crack, or induce cracking in the GaN substrate surface. The first step towards doing this was to minimize the amount of SiO_2 by ensuring that the layer is thick enough to withstand the phosphoric acid etch without being significantly decreased in size as well as being mechanically stable enough to not bow under the weight of the

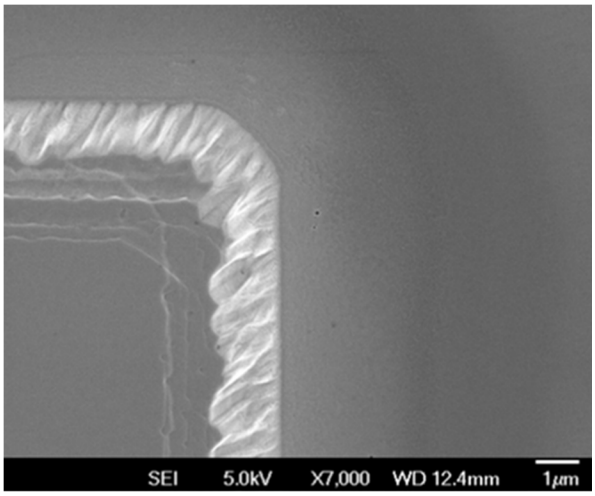

Fig. 5. A planview SEM image example of a sidewall with a slightly compressive mask. The lower left is the mesa surface. The sidewalls are not perfectly smooth; however they are continuous and substrate cracking is greatly reduced.

polycrystalline GaN deposited on top of it. Currently, 500nm has been sufficient. The SiN_x layer then must make up for the difference being 3µm. The increase in its thickness further emphasizes the need for it to remain intact.

Simply reducing the amount of SiO_2 did not fully alleviate the stress issues. To reduce the stress further, the deposition parameters of the PECVD-deposited SiN_x are being investigated. It is desirable to have a compressive residual stress in the film such that when it heats and tensile strain is induced, the magnitude of stress must first reduce before increasing again. There are a few strategies for controlling stress in PECVD deposited films, but for SiN_x the most effective has been shown to be adjusting the deposition power frequency. This can be done by adding a low frequency (LF) power supply in conjunction with the high frequency (HF) power supply and to alternate between a HF and LF plasma in cycles. Adding a LF plasma creates physical sputtering of the film from the ions since they are able to respond to the slower switching and move under the bias as opposed to the HF situation. Therefore, increasing the LF plasma time in the cycle increases the compressive stress of the film since the sputtering creates a film that is densely packed in on itself [15].

Initial work on this has been very promising. Even a small addition of LF power has resulted in much smoother sidewalls and has visibly reduced substrate cracking. This is shown in figure 5. In addition to this, the mask itself was fully intact when coming out of the MBE which hadn't been seen in previous instances. More study is being done on this by further increasing the LF power percentage and including a thin sputtered SiN_x layer at the base of the mask.

CONCLUSIONS

This work demonstrates the feasibility of PAMBE-enabled SNS-SAG to be a suitable method for fabricating a variety of power devices, including diodes and transistors. The ability of this technique to produce smooth, low-defect sidewalls significantly reduces the effect of leakage current and greatly improves overall performance. Further work is underway to produce thicker mesas for higher voltage functionality. Promising results have been shown indicating that stress engineering is the key to making thick SNS-SAG layers practical.

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ACRONYMS

SNS: Silicon Nitride Shadowed
SAG: Selective Area Growth
PAMBE: Plasma-Assisted Molecular Beam Epitaxy
GaN: Gallium Nitride
ICP-RIE: Inductively Coupled Plasma Reactive Ion Etching
SEM: Scanning Electron Microscopy
CL: Cathodoluminescence
C-AFM: Conductive Atomic Force Microscopy
XPS: X-ray Spectroscopy
SBD: Schottky Barrier Diode
DiVSET: Dielectric Vertical Sidewall-Appended Edge Termination
SiN_x: Silicon Nitride
SiO_2: Silicon Dioxide
CTE: Coefficient of Thermal Expansion
LF: Low Frequency
HF: High Frequency