Rounded base corners in SiC trenches for power MOSFETs

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Abstract

SiC trench structures, which find increasing use in power devices such as UMOSFETs, require optimization of their geometry for best performance. Modelling shows that rounded corners with radius of curvature of 185 nm yield a 36% reduction in localized electric fields compared to right-angled trench corners. A 2-step plasma etch process demonstrating trench corner rounding has been developed to enable efficient power SiC devices with more reliable and efficient performance.

INTRODUCTION

Next generation SiC MOSFET devices will incorporate trenches into their gate structure, eliminating the efficiency-limiting JFET resistance and improving inversion channel mobility[1,2,3]. Trenches in SiC, of widths ranging 0.5-3µm and depths 1-3µm, must be plasma etched, with a key design aspect being the cross-sectional shape of the trench. MOSFET gates must maintain strong electric potentials, where field lines can 'crowd' around sharp features such as trench corners and micro-trenches. This field crowding increases local field strength and reduces the breakdown voltage of the device, limiting reliability and maximum efficiency, as well as increasing costs. Optimization of the etch process can eliminate micro-trenching, providing a flat-based trench with improved characteristics compared to other, micro-trenched device structures. Few previous reports have explored beyond micro-trench elimination and assessed rounding the trench base corners. This work presents simulations of trenches with round corners and their effect on field strength. Finally, a novel plasma etching method successfully achieves *in-situ* production of rounded corners in SiC trenches.

METHODS

Sentaurus TCAD simulations of SiC trench MOSFET structures investigated the effect of trench corner curvature on the electric field profile. A trench MOSFET structure, Fig. 1(top), was designed with a drift region doping of $1x10^{16}$ cm^{-3} shown in Fig. 1(bottom). The radius of curvature of the trench bottom was varied, whilst maintaining the depth & position of the trench. This device was then simulated under reverse bias conditions of V_{ds} = 500 V, 750 V & 1000 V, with the maximum electric field in the SiC region recorded at each voltage. For comparison, an identical reverse bias simulation was completed at each of the three bias points for a trench of same depth and width but with sharp right-angled corners.

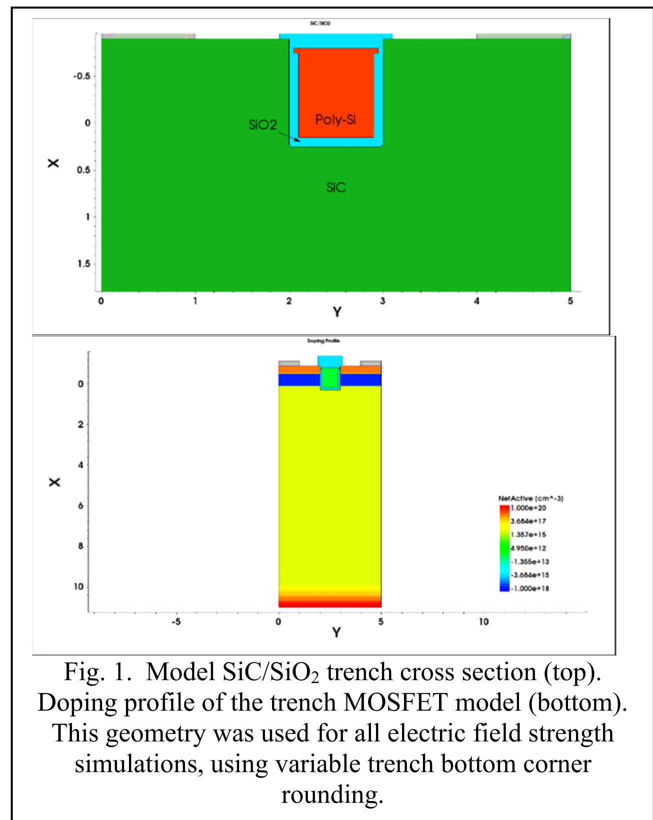

Fig. 1. Model SiC/SiO_2 trench cross section (top). Doping profile of the trench MOSFET model (bottom). This geometry was used for all electric field strength simulations, using variable trench bottom corner rounding.

A novel etch process was developed to fabricate a SiC trench with rounded base corners, consisting of two steps[4]:

1) Initial etch: fast etch, resulting in a trench with steep side-walls & flat base.
2) Rounding step: passivation-rich etch, tuned specifically to round the base corners

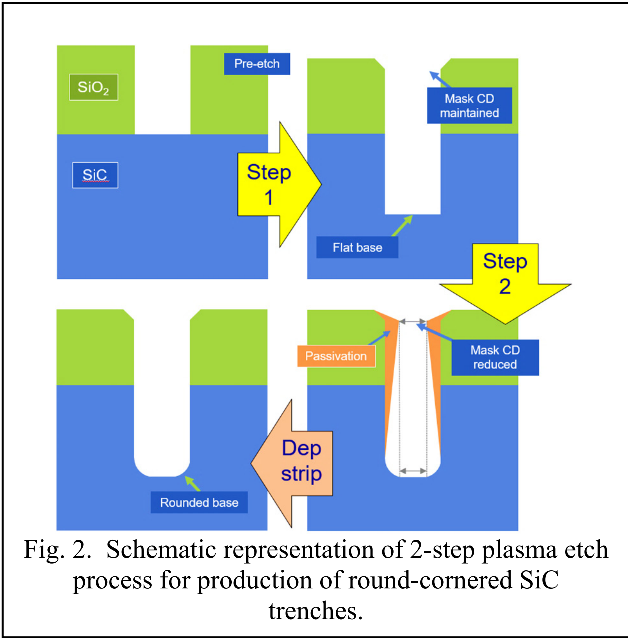

Fig. 2. Schematic representation of 2-step plasma etch process for production of round-cornered SiC trenches.

Fig. 2 shows a schematic representation of this approach, where step 2 was critical to rounding the corners of the square trench profile produced by step 1. Step 2 relies on passivation build-up that reduces the opening at the top of the trench as the step duration progresses. Owing to the directionality of the SiC etch process, this reduced opening translated to a reduced width of etch progression at the base of the trench. To smoothly vary the side-wall profile from vertical on the upper part of the trench to flat at the base, the rate of passivation build-up was carefully controlled throughout.

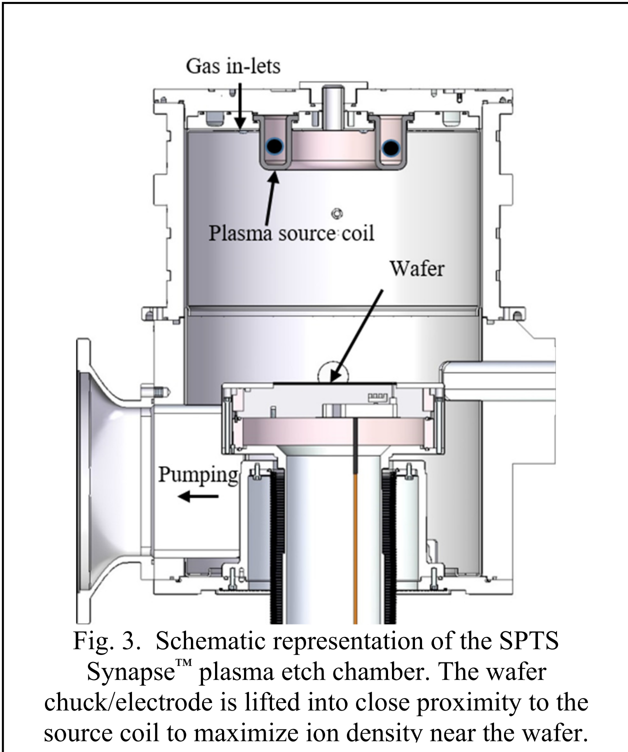

Fig. 3. Schematic representation of the SPTS Synapse™ plasma etch chamber. The wafer chuck/electrode is lifted into close proximity to the source coil to maximize ion density near the wafer.

This 2-step etch was performed on SiC wafers in the SPTS Synapse™ module (shown in Fig. 3), which is ideally suited to etching SiC and other hard materials owing to its high-density plasma. The wafer can be moved into close proximity to the plasma source, maximizing the availability of high energy ions to produce an anisotropic etch with high rate.

SIMULATION & ETCH RESULTS

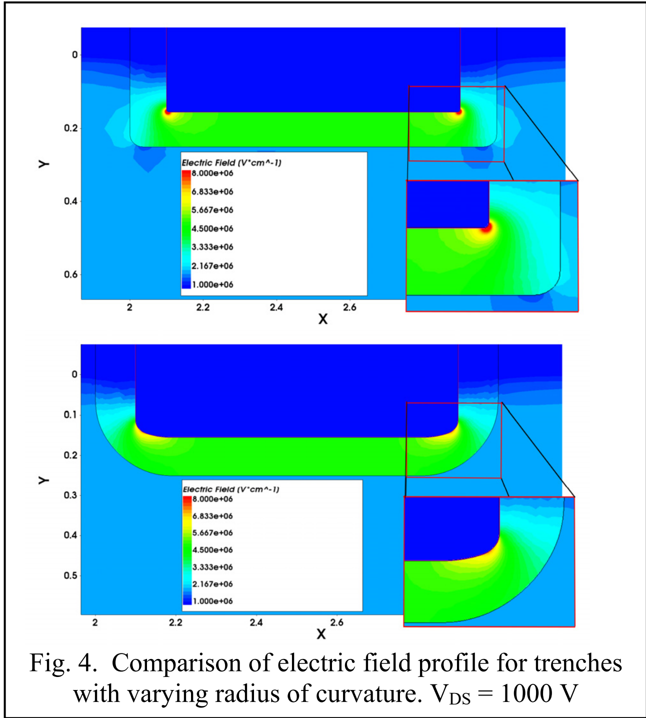

Fig. 4. Comparison of electric field profile for trenches with varying radius of curvature. V_{DS} = 1000 V

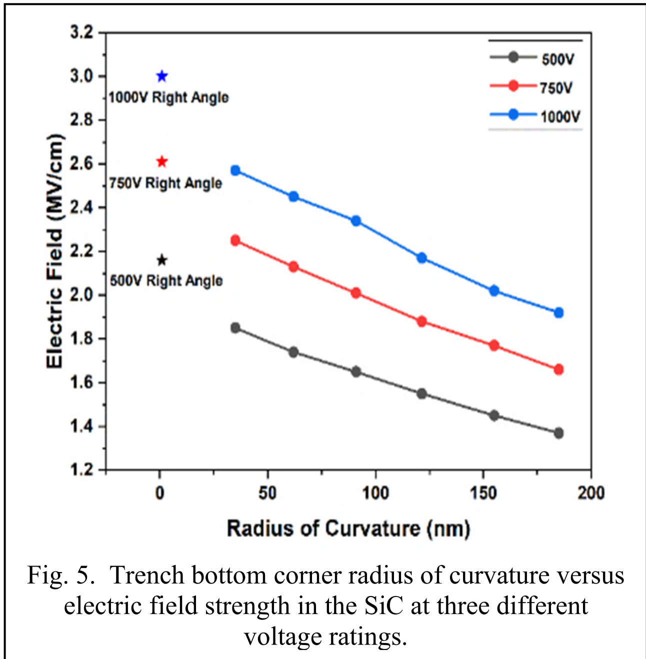

Fig. 5. Trench bottom corner radius of curvature versus electric field strength in the SiC at three different voltage ratings.

Device simulations (Fig. 4) show strong electric fields gathered around the corners of the trench, with the highest strengths found in the SiO_2 layer formed over the sidewalls and base of the SiC. The trench with low radius has sharper SiO_2 corners, causing higher field crowding and a higher peak electric field value.

Not limited to the SiO_2, Fig. 5 shows maximum field strengths in the SiC, with a linear decrease of ~0.1 MV/cm per 30 nm of increased radius of curvature. This rate of decrease in field strength is consistent across all three bias points. By increasing the radius of curvature of the trench etch by 100 nm, a decrease of 0.32 MV/cm, 0.4 MV/cm and 0.43 MV/cm in field strength is observed at V_{ds}= 500 V, 750 V and 1000 V, respectively. This equates to a ~17% decrease in field strength at all bias points simulated. When comparing the trench with the largest radius of curvature simulated (185 nm) with a trench possessing a right-angle corner, a field decrease of 36% was observed at all three V_{ds} values. These results carry even more significance when the magnitude of the electric field is considered. At V_{ds} = 500 V, a drop of 0.78 MV/cm field strength in the SiC would result in a drop of 2 MV/cm in the gate oxide due to Gauss' law[1].

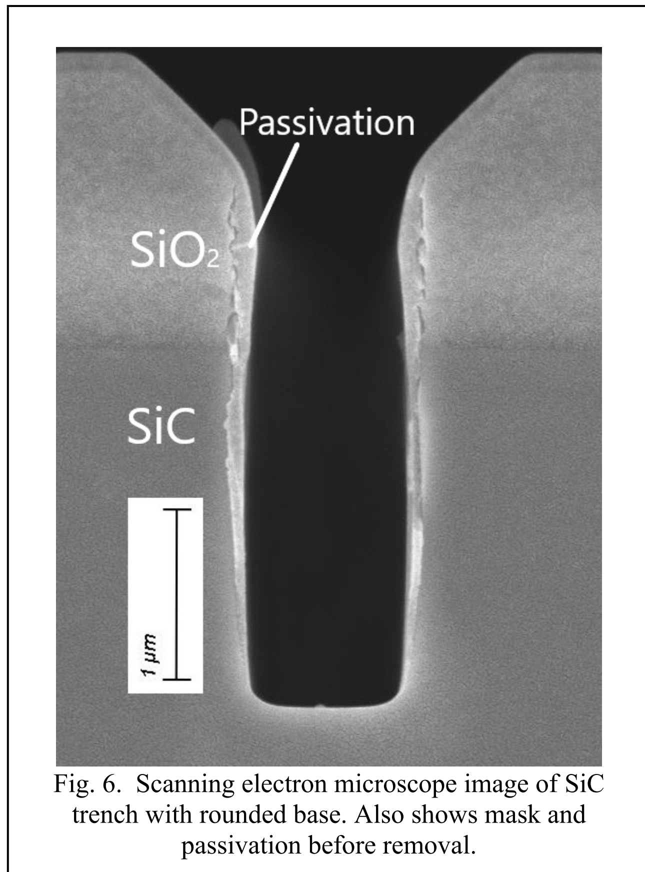

Fig. 6. Scanning electron microscope image of SiC trench with rounded base. Also shows mask and passivation before removal.

Fig. 6 shows a cross-sectional image of a SiC trench with rounded base corners (corresponding to the schematic in Fig. 3: bottom right). The passivation present on the sidewalls of the trench and mask remains post-etch and can be removed by wet acid treatment post-etch (see Fig. 6). Typical 2-step etches proceed with an overall etch rate of 500 nm/min, 3.5:1 selectivity to the SiO_2 mask and a cross-wafer depth non-uniformity of ±3% at an edge exclusion of 4 mm. The corners in the trench shown have a radius of ~250 nm, the depth is 2.1µm, the trench top width is 1.1µm and the side-wall profile angle is 88.8°.

Fig. 7 presents two trenches (on the same wafer in approximately the same location) that have had their mask removed by acid treatment. Some passivation remains due to the non-optimized wet chemical process. The plasma etch process is capable of etching over a broad range of starting trench widths, with only minor variations in characteristics between differing sizes. Trenches of width 1.0 and 1.3 µm (left and right in Fig. 7) have depths of 2053 and 2152 nm respectively, a RIE lag range of ±2.4%. RIE lag and other characteristic variations may increase as the aspect ratio increases at small CDs, but over this range the results are maintained. Notably, the base corners are smoothly rounded with similar radii at both 1.0 and 1.3 µm CD of around 250 nm.

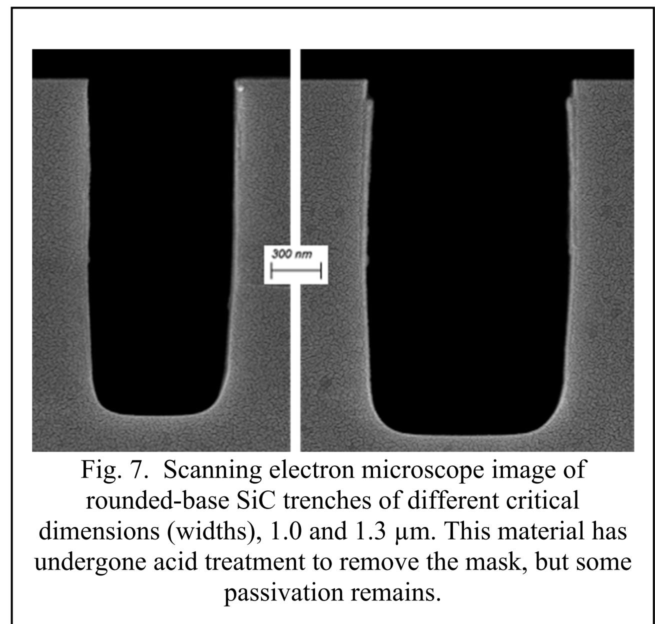

Fig. 7. Scanning electron microscope image of rounded-base SiC trenches of different critical dimensions (widths), 1.0 and 1.3 µm. This material has undergone acid treatment to remove the mask, but some passivation remains.

Fig. 8 shows a comparison of the resulting trench base geometries of different SiC etch process types; achieving the large radius of curvature shown in the bottom image is made possible by the 2-step etch process presented here. The simulation results thus suggest this approach would be suitable to produce SiC trenches for next generation MOSFET devices.

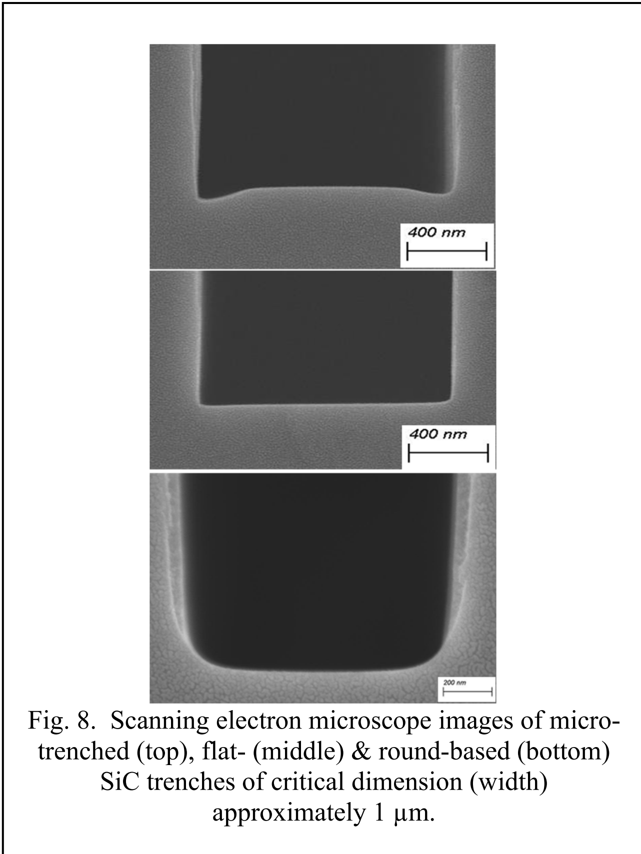

Fig. 8. Scanning electron microscope images of micro-trenched (top), flat- (middle) & round-based (bottom) SiC trenches of critical dimension (width) approximately 1 µm.

CONCLUSIONS

Sentaurus TCAD modelling predicts that round-based SiC trenches with corners of increased radius will have improved MOSFET reliability performance compared to square-cornered trenches. A 2-step plasma etch process has been developed to produce trenches with these smooth, large radius corners. Rounded trench MOSFETS can hence be fabricated, which should yield power devices with reduced gate electric fields, improving reliability and efficiency in the next generation of power devices.

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ACRONYMS

MOSFET = metal oxide semiconductor field effect transistor
JFET = field effect transistor current density
TCAD = Technology Computer Aided Design