

Bilayer N-metal Lift-off Process on Thick DBRs Mesa for Low-Threshold VCSELs

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Abstract

To reduce VCSEL threshold current for better power efficiency and reduced heat dissipation, one approach is to enhance cavity quality factor “Q” by increasing the number of P-DBR pairs for lower mirror loss. However, the increased p-DBR mesa height results in fabrication challenges. A consequential failure encountered in VCSEL N-metal bilayer lift-off process is reported. The failure mechanism is analyzed in detail, and a modified recipe for stable bilayer N-metal lift-off process is presented.

INTRODUCTION

850nm GaAs VCSELs are widely employed as optical transmitters in short-reach optical interconnects due to low power and high speed [1]. Meanwhile, VCSELs also have increasing applications in 3D sensing, Lidar and 5G [2]. In 2016, we demonstrated 850nm oxide-confined VCSEL with 57Gb/s error-free data transmission for data center application [3]. The epitaxial layer structure, from bottom to top, consists of n-doped AlGaAs DBRs, 0.5- λ active region containing InGaAs/AlGaAs multiple quantum wells (MQW), and a total of 20 pairs of p-doped AlGaAs DBRs [4].

In order to further lower the VCSEL threshold for better power-efficiency and less heat dissipation, one approach implemented is to add more P-DBR pairs. But adding more DBR pairs also lead to new fabrication challenges in various process steps due to the increased mesa height. In this work, we report a failure mechanism and a stable solution to it in a bilayer N-metal lift-off process for a modified VCSEL structure with 23 pairs of p-doped AlGaAs P-DBRs and 1- λ active region containing InGaAs/AlGaAs MQWs.

BASELINE N-METAL PROCESS

In our baseline high-speed VCSEL fabrication process, N metal lithography and deposition are performed following P-metal deposition, mesa etch and wet oxidation [5]. The N-metal lithography utilizes a Cap-On Bilayer Lift-Off Process. A cross-section drawing for an ideal lithography before metal deposition is illustrated in Fig. 1 (a). Specifically, multi-layer PMGIs are coated first for mesa coverage and planarization (here “coat” includes baking for simplified expression). Then imaging resist such as AZ 1505 is coated for pattern transfer. AZ1505 in the defined N-metal region is first exposed and developed. Afterwards, repeated DUV flood exposures and developments in 101A developer are performed to develop PMGI and achieve enough undercut. In this process the PMGI thickness is much more than the target undercut, which requires

a near-anisotropic development of PMGI film. Fig. 1 (b) shows

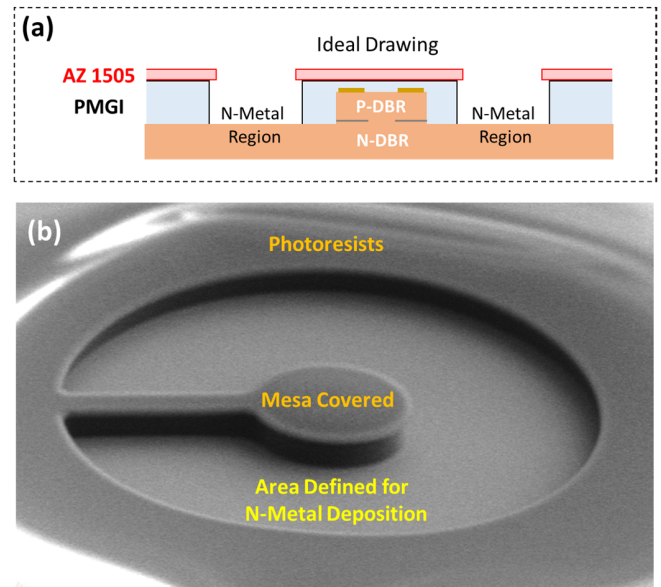


Fig. 1. (a) Ideal case for N-metal lithography. (b) Stable N-metal lithography in the past. Mesa height was 4.1 μm .

an SEM image of our previous successful and stable N-metal lithography results when the mesa height including P-metal was 4.1 μm (20 P-DBR pairs and 0.5- λ cavity).

PROBLEM ILLUSTRATION AND DIAGNOSIS

Recently, in the attempt to reduce VCSEL threshold current, more P-DBR pairs are added to VCSEL epilayers and the mesa height including P-metal increases to 4.9 μm (23 P-DBR pairs and 1- λ cavity). So, in the N-metal lithography, PMGI thickness is increased to approach 5 μm accordingly, beyond which the lithography resolution cannot be guaranteed. Then, AZ1505 is coated and patterned. During mask contact in Karl Suss MJB3 Aligner, exposure for AZ1505, and development of AZ 1505 in diluted AZ developer, the photoresists protecting the mesa keeps intact. However, during subsequent repeated DUV Flood exposures and developments in 101A developer, it is observed that the photoresists covering the mesa is attacked starting at the center point of the mesa, gradually leaving a hole in the center as shown in Fig. 2 (a). It is unexpected because after the previous step, AZ1505 on top of PMGI still covers the mesa and the total photoresist thickness actually has the highest value in the center of the mesa.

With DOE experiments and more characterizations during the process, the failure mechanism is identified as shown in Fig.

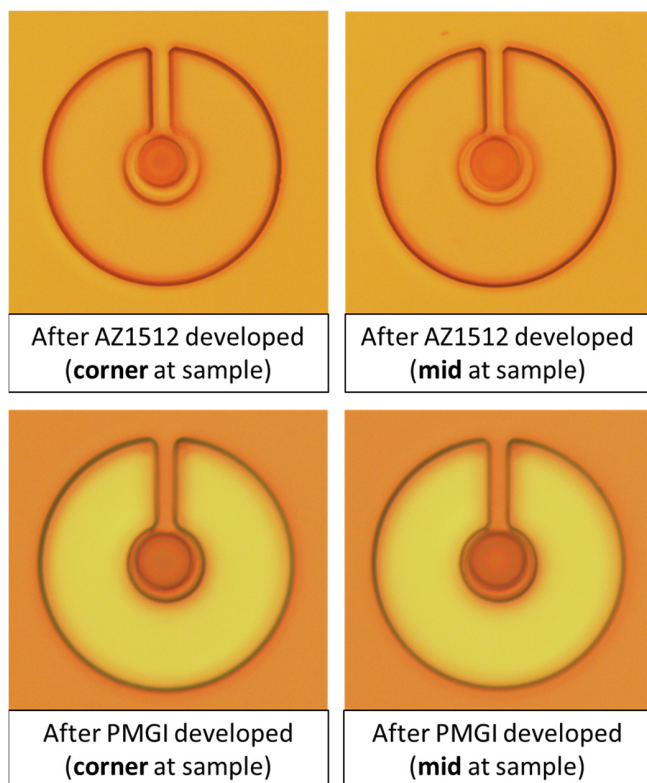


Fig. 3. Successful lithography on DOE structures (GaAs without epitaxial layers or p-metal). Ring interference patterns can reflect the slight difference of thickness and profile of the photoresist, at different regions of the $1.2 \times 1.2 \text{ cm}^2$ sample.

2 (b-1) - (b-4). Surface profile measurement in this work is performed with a Bruker Dektak XT Surface Profiler. As shown in Fig. 2 (b-1), after multi-layer PMGI is coated ($4.93 \mu\text{m}$), the PMGI surface still has a protruding hill shape in the mesa region with at least $1.23 \mu\text{m}$ height difference in the center. Then, after the subsequent AZ1505 coating ($0.76 \mu\text{m}$ thickness on plain GaAs), the AZ1505 at the top of “hill” on mesa is much thinner than plain region, as shown in Fig. 2 (b-2). During the imaging exposure using quartz mask, the contact pressure is focused on the top of “hills” where AZ1505 is thin. Subsequently during the AZ1505 development in diluted AZ developer, the dark erosion further reduces the AZ1505 thickness. At this stage, although the photoresists look intact, the AZ1505 on the top of “hill” is nearly deplete, as shown in Fig. 2 (b-3). Finally, during repeated flood DUV exposures, PMGI developments and rinses, the AZ1505 on the top of “hill” is depleted by dark erosion and 101A developer starts to attack PMGI starting at the center of mesa, as shown in Fig. 2 (b-4).

It is also found that the corner devices on the $1.2 \times 1.2 \text{ cm}^2$ samples fails first during the repeated flood DUV exposures, PMGI developments and rinses, with photoresist attacked from the center. The reason is the slight mesa height difference between middle devices (lower) and corner devices (higher) due to the previous dry-etch step. The photoresist spin coating and development uniformity can also contribute to this observation.

SOLUTION AND RESULTS

After the failure mechanism is identified, three directions of improvements are proposed. First of all, the thickness of the imaging photoresist on top of PMGI needs to be increased. Secondly, the imaging photoresist needs to have a minimum dark erosion rate. Thirdly, the choice of developer should also minimize the dark erosion.

Therefore, in the modified process, AZ1512 is used as the imaging photoresist, which features higher thickness than AZ1505, very high development rate and minimized dark erosion. What is more, AZ 917MIF is used as the developer, which features low surface tension and high development rate without sacrificing selectivity.

The modified process stably solve the problem for all the devices on $1.2 \times 1.2 \text{ cm}^2$ N-doped GaAs DOE samples and formal samples with devices. The GaAs DOE samples are prepared with mesa structures with the same diameter and height compared to actual devices, but without epitaxial layers or p-metal. Fig. 3 demonstrates the lithography results on DOE sample with the modified recipe. The top two OM (optical microscope) pictures are taken after AZ1512 is patterned. Since the top surface of GaAs mesa here is flat and the photoresist on top has a spherical surface, ring interference pattern are created by the reflection of light. Thus the slight differences of thickness and profile of the photoresist between middle “device” and corner “device” can be visualized. Also, it is observed that the ring interference pattern on each GaAs mesa changes slowly after repeated DUV flood exposures and developments of PMGI, which corresponds to the unwanted erosion of AZ1512 in PMGI developer. The bottom two OM pictures shows the results when PMGI are fully developed, while the mesa is still protected well by photoresist.

Fig. 4(a) shows the OM picture after a successful N-metal lithography with formal devices. The $4.93 \mu\text{m}$ PMGI is fully developed with enough undercut. Meanwhile the photoresists that cover the mesa are intact. Fig. 4(b) shows the OM picture after N-metal deposition and successful Lift-off. Fig. 4 (c) shows the SEM picture correspondingly, with N-metal labeled. After annealing, the TLM results of N metal contact demonstrate Ohmic contact with low resistance. Thus, it is proved that the modified N-metal process is successful.

CONCLUSION

For increased pairs of P-DBR in VCSEL epi structure, a failure mechanism in bilayer N-metal lift-off process is identified. Then a modified process that stably solve the problem is presented.

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ACRONYMS

VCSEL: Vertical Cavity Surface Emission Laser
DBR: Distributed Bragg reflector
SEM: Scanning Electron Microscopy

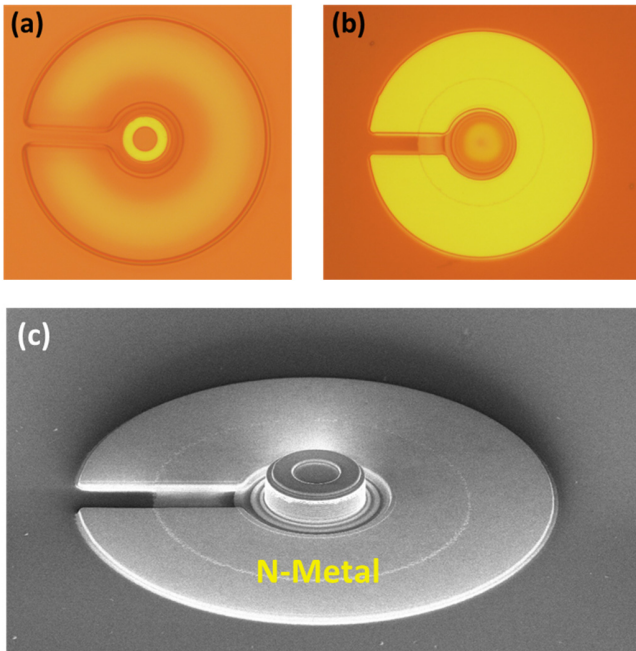


Fig. 4. (a) A successful lithography with the modified process and (b) subsequent N metal deposition and liftoff. (c) SEM picture of the successful N-metal Results

