Hole Injection Effect and Dynamic Characteristics Analysis of Normally-Off p-GaN HEMT with AlGaN Cap layer on Low Resistivity SiC substrate

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Abstract

p-GaN HEMT with AlGaN cap layer was grown on a low-resistance SiC substrate. The wide band gap material AlGaN as the cap layer, which can effectively suppress the holes injection and achieve the purpose of improving the gate reliability. In addition, we chose a zero-degree angle and low-resistance SiC substrate, which not only greatly reduces the lattice dislocation defects caused by the heterogeneous junction, but also greatly reduces the overall cost. The device shows the nice gate voltage swing of 18.5V (@I_{GS}=1mA/mm) and Off-state breakdown voltage of 763V. Especially, the dynamic characteristics and hole injection behavior was analyzed by pulse measurement, which caused Ron increasing and V_{TH} shifting under the gate lag effect.

INTRODUCTION

GaN power transistors have become one of the key devices in high-power and high-efficiency power conversion systems, mainly using material properties such as wide band gap 、 high mobility and high electric breakdown field. In order to achieve the device in normally off operation, various approaches such as the gate recessed structure [1-3], fluorine ion treatment [4], and a p-type GaN cap layer have been reported [5]–[7]. GaN power transistors have become one of the key devices in high-power and high-efficiency power conversion systems, mainly using material properties such as high breakdown voltage, fast switching speed and low on-resistance. However, in commercial p-GaN HEMTs, device gates can be divided into ohmic contacts or Schottky contacts. Ohmic gates such as gate injection transistors (GIT), and Schottky gates have lower forward gate leakage current is mainly due to a reverse Schottky diode at the junction of the metal and p-GaN. At the same time, the Schottky gate p-GaN HEMT also exhibits a time-dependent gate breakdown voltage (TDGB), but the gate operating voltage is limited to 6~7 V. Therefore, many groups are developing methods to increase the maximum value so that it can be used in a wider gate bias operating range. Under positive bias, the gate breakdown of p-GaN HEMT can be attributed to the high electric field concentrated at the metal/p-GaN interface. Different from the TDDB performance of Si and SiC power MOSFETs, the TDGB behavior of p-GaN HEMTs usually shows a positive correlation with the temperature coefficient, which means that high-energy carriers are accelerated by impact ionization or hot electron bombardment in a high electric field. Therefore, one of the methods to improve the reliability of the gate is to make structural or process changes at the metal/p-GaN junction. On the other hand, many studies have analyzed the physical mechanism of dynamic resistance change, which is mainly caused by hot electron injection on the surface and defects in the buffer layer. There are many ways to produce these defects, such as: carrier vacancy, lattice dislocation and impurities. On the other hand, GaN devices are mostly operated under high-frequency and high-power operating conditions, so the characteristics of the device during high-temperature operation are also important. In particularly, there are two different substrates in the p-GaN HEMT, namely GaN-on-Si and GaN-on-SiC. However, compared with GaN-on-Si HEMT, GaN-on-SiC HEMT is expected to be a good choice for high-power switching components due to its high thermal conductivity, low resistivity, and high-voltage capability. Another advantage of using a SiC substrate is its lower lattice mismatch of ~3% for GaN (that of Si is ~17%). Therefore, a low-resistance and zero-degree SiC substrate, which not only has the advantages of the above-mentioned GaN on SiC, but also has a lower price than high resistivity SiC substrate. Finally, we combine the AlGaN cap layer and low resistivity SiC substrate on the p-GaN HEMT, which were published in journal paper, respectively [8-9].

EXPERIMENTAL PROCEDURES

In this work, the AlGaN/p-GaN/AlN/AlGaN/GaN HEMT was grown on 6-inch low resistivity SiC substrate by MOCVD. For the epitaxial structure is presented in Fig. 1(a), an undoped GaN channel layer with a thickness of 300 nm was grown on an undoped AlGaN/GaN buffer/transition layer with a thickness of 4 µm. Subsequently, a $Al_{0.25}Ga_{0.75}N$ barrier layer with a thickness of 15 nm and a p-type GaN layer with a thickness of 100 nm were grown. Finally, a $Al_{0.2}Ga_{0.8}N$ was grown on the p-GaN layer with a thickness of 10 nm. For the device fabrication, the p-GaN etching of $Cl_2/BCl_3/SF_6$ based inductively coupled plasma and the AlN layer as an etching stop layer. The ohmic contacts were prepared by electron beam evaporation and Ti/Al/Ni/Au (25/120/25/150 nm) were stacked on the device sequentially. Then, both devices were annealed by RTA system at 875 ◦C for 30 s in N_2 ambient. Finally, a Ni/Au (25/120 nm) gate metal stack is deposited and 100 nm of SiO_2 was passivated.

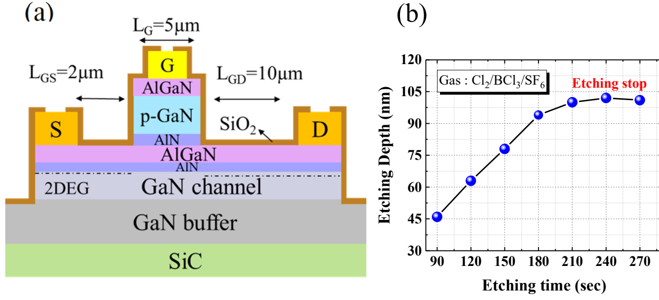

Fig. 1(a) Cross sectional schematic of p-GaN gate HEMT, (b) the etching stop technique and p-GaN profile by AFM analyze.

RESULTS AND DISCUSSION

Fig 2(a) and (b) shows the log-scale transfer (I_{DS}-V_{GS}) and output (I_{DS}-V_{DS}) characteristics of the device. As shown in Fig3(a), the off-state current was 5×10^{-5}mA/mm at $V_{GS} = 0$ V. Additionally, the threshold voltage (V_{TH}) value 1.5 V. The corresponding maximum drain current density (I_{Dmax}) values and R_{on} were 210 mA/mm and 20 Ω · mm, respectively.

To observe the hole injection effect during the gate operation, I_{GS}-V_{GS} measurement was shown in Fig3(a). The device exhibits the large gate operation voltage under the forward bias and the gate turn on voltage (V_{GS_ON}) of 18.5V was defined at V_{GS}=1mA/mm. The device obtains the better gate behavior due to the thicker and higher barrier height, which may suppress the carrier injection effectively. In Fig3(b), the device shows a high Off-state breakdown voltage of 763V.

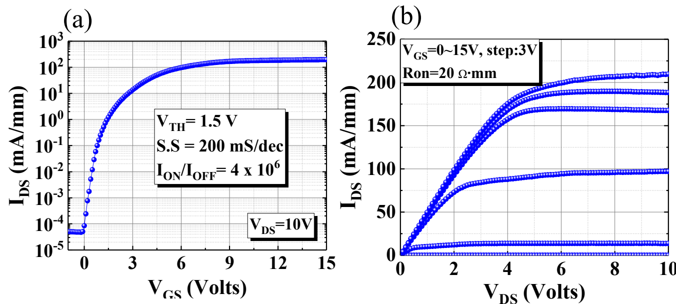

Fig. 2. DC characteristics of device with $L_{GS}/L_G/L_{GD}/W_G$ = 2/5/10/100 μm. (a) Transfer characteristic. (b) Output characteristic.

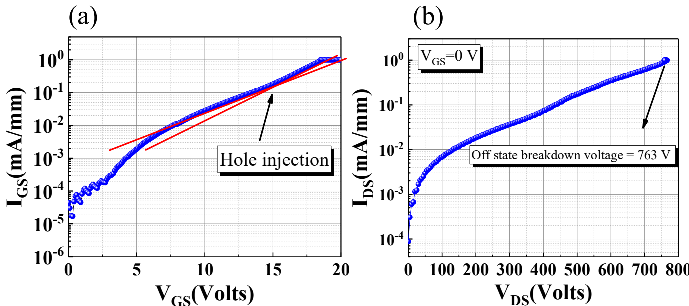

Fig. 3. (a) I_{GS}-V_{GS} characteristic and (b) Off-state breakdown voltage measurement of device.

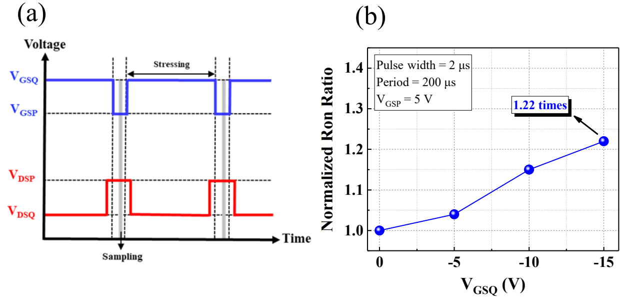

Fig. 4. (a) Condition of pulse measurement and (b) gate lag characteristic.

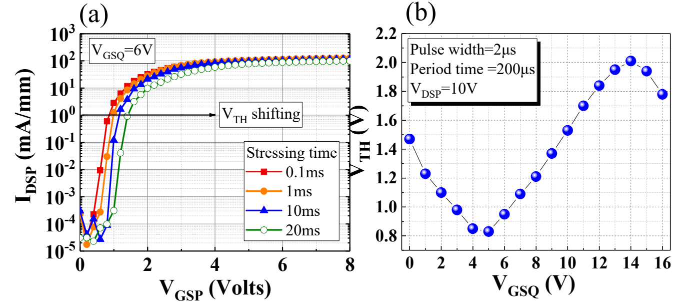

Fig. 5. (a) Dynamic transfer characteristics measured at with different stressing times and (b) V_{TH} shifting with different V_{GSQ}.

In this work, we use pulse measurement to analyze the hole injection effect and dynamic characteristics of the device under different stress voltage (V_{GSQ}) and stressing times. The operation condition and gate lag measurement were shown in Fig. 4(a), (b), respectively. There are two bias conditions that must be considered: pulse voltage (V_{GSP}, V_{DSP}) and quiescent voltage (V_{GSQ}, V_{DSQ}). During the measurement, when the pulse voltage switched to the quiescent voltage rapidly with a 2 μs pulse width and 200 μs period, and the V_{GSQ} was swept from 0 to −15 V in increments of −5 V. The device shows the dynamic Ron of 1.22 times at V_{GSQ}= -15V.

In Fig. 5(a), the V_{TH} shift towards the positive direction under the V_{GSQ}=6 V when the stressing time increases in 0.1/1/10/20 ms, respectively. This phenomenon is causing by the enhanced electron injection from channel at higher V_{GSQ} and trapping at the p-GaN/AlN/AlGaN interface. Moreover, the V_{TH} shifting can be plotted in the pulse measurement, as shown in Fig. 5(b). When a V_{GSQ} is applied from 1V to 5V, the hole holes may accumulate at the p-GaN/AlGaN interface (see the schematic band diagrams in Figure. 6(a)), or trap states in the AlGaN/GaN interface, increasing 2DEG density temporarily and causing negative shifting of V_{TH}. When a V_{GSQ} is applied from 5V to 15V, V_{TH} shift towards the positive direction. This phenomenon can be explained that some injected electrons will be captured by the electron traps in the p-GaN/AlGaN interface, and the trapped electrons cannot escape immediately (see the schematic band diagrams in Figure. 6(b)). Afterward, the stress voltage is larger than 15V, the hole injection is turned on and inject to the p-GaN/AlGaN interface which recombine the trapping electrons (see the

schematic band diagrams in Figure. 6(c)), so the V_{TH} shifting trend reverse again [10-14].

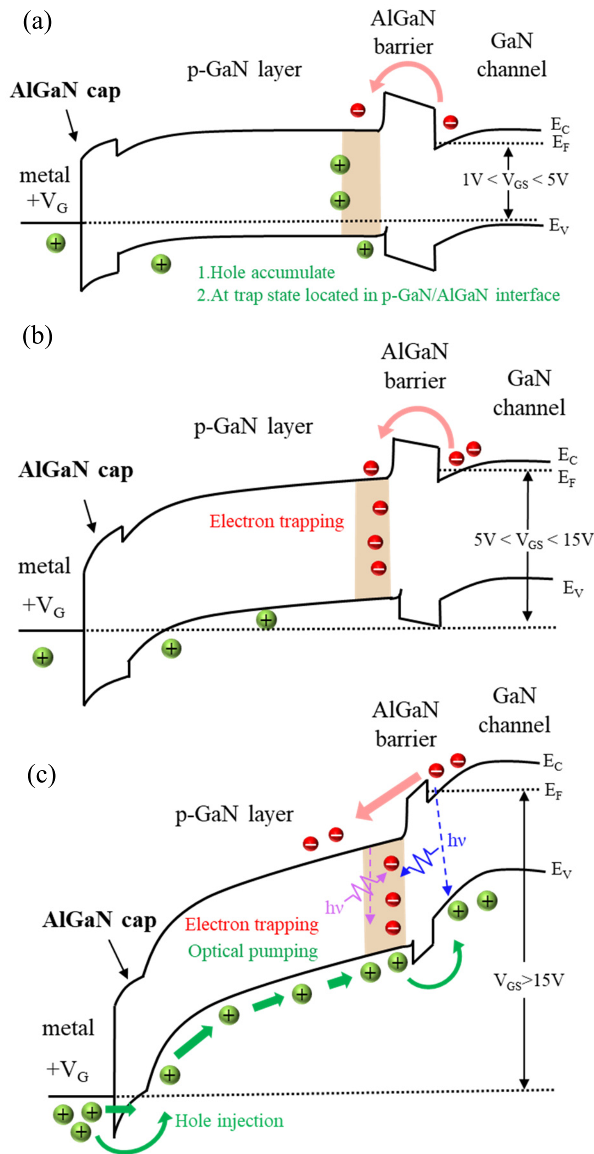

Fig. 6. Band diagram of p-GaN HEMT at (a) 1V< V_{GSQ} <5V, (b) 5V< V_{GSQ} <15V (c) V_{GSQ} >15V.

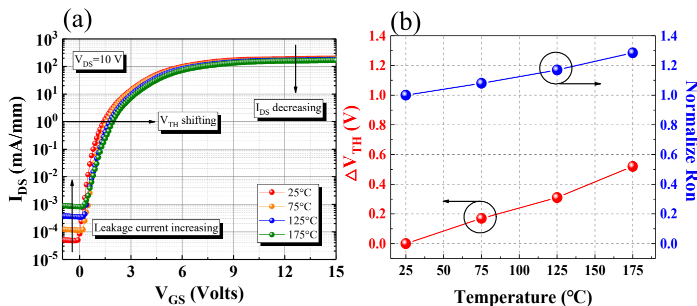

Fig. 7. (a) I_{DS}-V_{GS} characteristics of device from 25 to 175°C, and (b) value variation of V_{TH} and R_{ON}.

To analyzed the thermal characteristics of the device, I_{DS}-V_{GS} characteristic was measured under 25˚C to 175˚C with a 50˚C step, as shown in Fig. 7(a). The device shows V_{TH} shifting less than 0.3V and Ron increasing to 1.28 times up to 175˚C, as shown in Fig. 7(b). As the result, p-GaN HEMT on SiC substrate obtain a good thermal stability due to the high thermal dissipation ability. Finally, the distribution of V_{TH} and R_{ON} characteristics for 30 devices were measured in Fig. 8. For the device, the mean value of V_{TH} and R_{ON} are 1.5V and 20 Ω · mm.

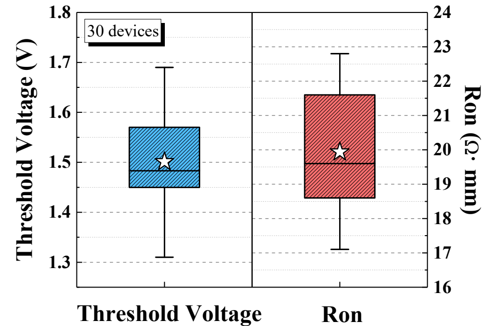

Fig. 8. V_{TH} and Ron distribution of 30 devices.

CONCLUSIONS

In this work, AlGaN cap on the p-GaN layer is to reduce the hole injection effect and make a large gate operation range. It is hoped that the gate driver of traditional silicon devices can be shared, and the operating safety voltage of the gate will be increased at the same time. In addition, we also grew p-GaN HEMT with AlGaN cap layer on a low-resistance SiC substrate, so that the GaN on SiC have a lower lattice defect density at the buffer layer position, improve heat dissipation performance and there are also lower prices.

REFERENCES

[1] W. B. Lanford, T. Tanaka, Y. Otoki, and I. Adesida, "Recessed-gate enhancement-mode GaN HEMT with high threshold voltage," Electron. Lett., vol. 41, no. 7, pp. 449–450, Mar. 2005, doi: 10.1049/el:20050161.

[2] T. Oka and T. Nozawa, "AlGaN/GaN recessed MIS-gate HFET with high-threshold-voltage normally-off operation for power electronics applications," IEEE Electron Device Lett., vol. 29, no. 7, pp. 668–670, Jul. 2008, doi: 10.1109/LED.2008.2000607.

[3] Q. Zhou et al., "7.6 V threshold voltage high-performance normally-off Al2O3/GaN MOSFET achieved by interface charge engineering," IEEE Electron Device Lett., vol. 37, no. 2, pp. 165–168, Feb. 2016, doi: 10.1109/LED.2015.2511026.

[4] Y. Cai, Y. Zhou, K. J. Chen, and K. M. Lau, "High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment," IEEE Electron Device Lett., vol. 26, no. 7, pp. 435–437, Jul. 2005, doi: 10.1109/LED.2005.851122.

[5] Y. Uemoto et al., “Gate Injection transistor (GIT)—A normally-off AlGaN/GaN power transistor using conductivity modulation,” IEEE Trans. Electron Devices, vol. 54, no. 12, pp. 3393–3399, Dec. 2007, doi: 10.1109/TED.2007.908601.
[6] S. Kaneko et al., “Current-collapse-free operations up to 850 V by GaNGIT utilizing hole injection from drain,” in Proc. IEEE 27th Int. Symp. Power Semiconductor Devices ICs (ISPSD), Hong Kong, May 2015, pp. 41–44, doi: 10.1109/ISPSD.2015.7123384.
[7] D. Marcon, Y. N. Saripalli, and S. Decoutere, “200 mm GaN-on-Si epitaxy and e-mode device technology,” in IEDM Tech. Dig., Washington, DC, USA, Dec. 2015, pp. 16.2.1–16.2.4, doi: 10.1109/IEDM. 2015.7409709.
[8] Chia-Hao Liu, Hsien-Chin Chiu, Hsiang-Chun Wang, Hsuan-Ling Kao, Chong-Rong Huang, “Improved Gate Reliability Normally-Off p-GaN/AlN/AlGaN/GaN HEMT With AlGaN Cap-Layer,” *IEEE ELECTRON DEVICE LETTERS*, VOL. 42, NO. 10, OCTOBER, 2021.
[9] Yu-Chun Huang, Hsien-Chin Chiu, Hsuan-Ling Kao, Hsiang-Chun Wang, Chia-Hao Liu, Chong-Rong Huang, Si-Wen Chen, “High Thermal Dissipation of Normally off p-GaN Gate AlGaN/GaN HEMTs on 6-Inch N-Doped Low-Resistivity SiC Substrate,” Micromachines 2021, 12, 509.
[10] Matteo Meneghini, “Technology and Reliability of Normally-Off GaN HEMTs with p-Type Gate”, Energies, 10, 153, 2017.
[11] T.-L. Wu, D. Marcon, S. You, N. Posthuma, B. Bakeroot, S. Stoffels, M. Van Hove, G. Groeseneken, and S. Decoutere, “Forward bias gate breakdown mechanism in enhancement-mode p-GaN gate AlGaN/GaN high-electron mobility transistors,” IEEE Electron Device Lett., vol. 36, no. 10, pp. 1001–1003, Oct. 2015.
[12] M. Tapajna, O. Hilt, E. Bahat-Treidel, J. Wurfl, and J. Kuzmik, “Gate reliability investigation in normally-off p-type-GaN Cap/AlGaN/GaN HEMTs under forward bias stress,” IEEE Electron Device Lett., vol. 37, no. 4, pp. 385–388, Apr. 2016.
[13] X. Tang, B. Li, H. A. Moghadam, P. Tanner, J. Han, and S. Dimitrijev, “Mechanism of threshold voltage shift in p-GaN gate AlGaN/GaN transistors,” IEEE Electron Device Lett., vol. 39, no. 8, pp. 1145–1148, Aug. 2018.
[14] Yuanyuan Shi, Qi Zhou, Qian Cheng, Pengcheng Wei, Liyang Zhu, Dong Wei, Anbang Zhang, Wanjun Chen, Bo Zhang, “Carrier Transport Mechanisms Underlying the Bidirectional V_{TH} Shift in p-GaN Gate HEMTs Under Forward Gate Stress”, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 66, NO. 2, FEBRUARY 2019.