

Improved RF Characteristics of AlGaN/AlN/GaN HEMT by using 3C-SiC/Si Substrate

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Abstract

This study investigates the AlGaN/AlN/GaN high electron mobility transistor (HEMT) epitaxial layers grown 3C-SiC/Si substrate. The SiC was grown between GaN Buffer layer and Si substrate. In the X-ray-diffraction, the lower FWHM value of SiC on Si HEMT shows less dislocation density. Furthermore, SiC on Si HEMT has a similar coefficient of thermal expansion (CTE) and lattice size with GaN, so it has fewer traps. Because of this reason, the characteristic of DC measurements has good performance. The $g_{m,max}$ values of SiC on Si HEMT is 147 mS/mm, $I_{DS,max}=598$ mA/mm and $R_{on}=4.63 \Omega \cdot mm$. High-Frequency measurement of SiC on Si operate on $V_{DS}=10$ V, $V_{GS}=-1.3$ V, and the current gain cutoff frequency of SiC on Si HEMT is 2.6 GHz Maximum Frequency of Oscillation of SiC on Si HEMT is 5.3 GHz. Therefore, GaN HEMTs SiC grown on Si substrate improve the lattice matching and improve the characteristic performance.

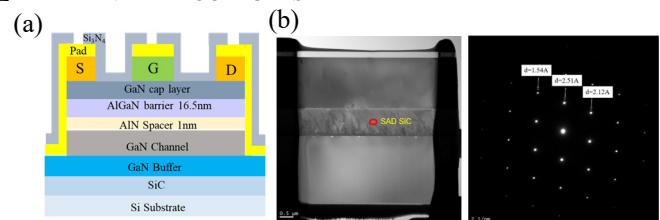
INTRODUCTION

At present, for GaN HEMT epitaxial growths there are three substrates of choice: silicon substrates (GaN on Si), silicon carbide substrates (GaN on SiC) and gallium nitride substrates (GaN on GaN). Silicon substrates with low cost and relatively mature manufacturing process are commonly used substrate materials in the industry. The energy band gap of Si is 1.12 eV, while the energy band gap of GaN is 3.4 eV. The gap between the energy gaps causes the problem of lattice dislocation during epitaxy. Therefore, in this paper, silicon carbide with an energy gap of 3.26 eV is used as the substrate grown on Si to effectively improve the Epitaxial quality. Due to the SiC between GaN and Si substrate, the cost can be effectively reduced, which solves the problem of high cost of the silicon carbide substrate, and the excellent thermal conductivity of the silicon carbide material is 4.9 W/cm-K, which reduces the spontaneous thermal effect of the component during operation. Produce GaN high electron mobility transistors (HEMTs) have superior material properties, such as high electron velocity, high breakdown field, and high operating temperature [1], so HEMTs develop in the high frequency and power device. The AlGaN/GaN heterostructures can be grown on sapphire, silicon, silicon

carbide, and native GaN substrates. Silicon is a common substrate material due to its low cost [2]. However, RF performance is still limited by different electron trapping effects, where DC-RF dispersion and memory effect are partly caused by traps located in the buffer [3]. Furthermore, GaN on Si has several disadvantages, e.g., high lattice mismatch density. SiC has been recently given renewed attention as a potential material for high-power and high-frequency applications requiring high-temperature operation. Some of the possible applications of SiC as a material for power electronics are for advanced turbine engines, propulsion systems, automotive and aerospace electronics, and applications requiring large radiation damage resistance. [4]. SiC is also a potential structural material in radiation environments because of its high thermal conductivity, chemical inertness [5]. MOVPE Growth of GaN films on Si (111) substrates has been studied. Thin 3C-SiC is found to be an effective intermediate layer for growth of single crystalline GaN films with flat surfaces [6].

In this letter, we also use Si substrate but grown 3C-SiC on Si substrate to reduce the lattice mismatch density and improve the electrical performance and reduce the leakage current. The SiC which is not only available for power devices but also be reliably used with microsensors and microactuators employed at high temperatures and in severe environments due to its excellent mechanical properties and chemical stability. Using Silicon as a substrate and growing a layer of SiC on it is used to reduce costs and improve electrical performance. In this paper, I will use SiC on Si substrate wafer compare with standard Si wafer which is called ST wafer to prove SiC on Si substrate wafer have good efficacy than ST substrate in DC performance, High-frequency, thermal image and low-frequency noise analysis measurement.

EXPERIMENTAL PROCEDURES



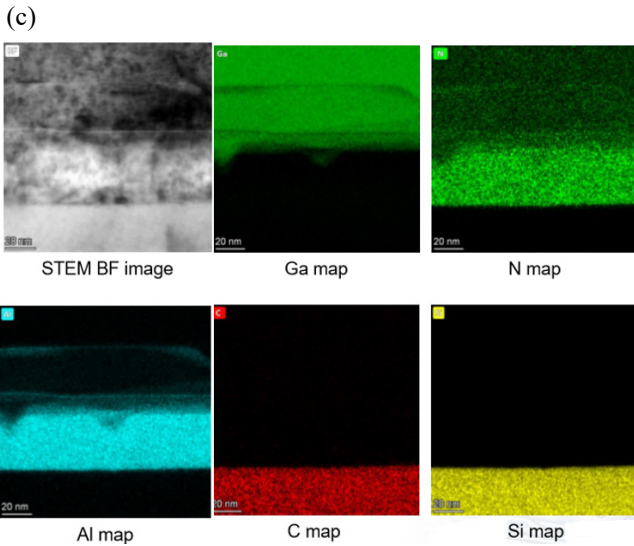
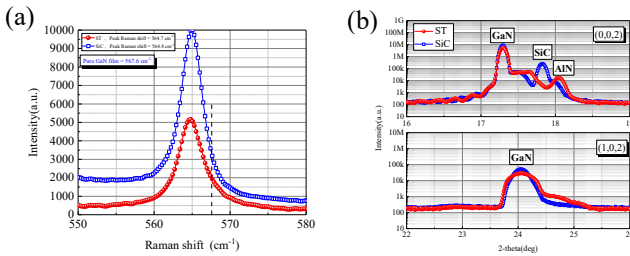


Fig.1(a) Cross sectional schematic of GaN HEMTs, (b) Cross sectional TEM image of SiC on Si HEMT, (c) Cross sectional EDS analysis of SiC on Si HEMT.

In this work, the 3C-SiC epitaxial layers was grown on 6-inch Si substrates by MOCVD. The layer stack consists of a 1- μm SiC, a 1500-nm GaN buffer layer, a 800-nm GaN channel layer, a 1-nm AlN spike layer, a 16.5-nm AlGa barrier layer, a 1-nm GaN cap, as shown in Fig. 1(a).

The first fabrication process was mesa isolation using $\text{Cl}_2/\text{BCl}_3/\text{Ar}$ by reactive ion etching (RIE). Second, source/drain ohmic contacts were formed using Ti/Al/Ni/Au (25/130/25/90 nm) by e-beam evaporation and subsequently alloyed at 900 $^\circ\text{C}$ for 30 s in N_2 ambient. Next, the Ni/Au gate metal which had been defined and Ti/Au was deposited as the pad. Finally, the device was passivated with Si_3N_4 by PECVD.

Fig. 1(b). is the Cross-sectional TEM image of SiC on Si HEMT. We can see the SiC between GaN buffer and Si substrate in the Fig. 1(b), and Fig. 1(b) also showed ring patterns with radii of 2.51 \AA , 2.12 \AA , 1.54 \AA corresponding well to the interplanar spacings of 3C-SiC. The TEM image and the discontinuity of the observed ring at certain angles suggest a preferential growth direction of the 3C-SiC grains in device [8]. Fig. 1(c). is the Cross-sectional EDS image of SiC on Si HEMT. The image shows the various elements contained in buffer layer and 3C-SiC intermediate layer.



(c)

	FWHM(002) (arcsec)	FWHM(102) (arcsec)	Dislocation(crew) (cm^{-2})	Dislocation(edge) (cm^{-2})	Dislocation(total) (cm^{-2})
3C-SiC/Si	415.8	908.28	3.47E+8	4.38E+9	4.727E+9
Si sub	631.44	1531.2	7.99E+8	1.24E+10	1.324E+10

Fig. 2 (a) Raman diagram, (b) X-ray-diffraction profiles of the GaN HEMT structure on SiC and Si substrates, (c) dislocation density of two devices.

RESULTS AND DISCUSSION

Fig.2(a) shows Raman measurement result among SiC on Si and ST substrates HEMT. Raman measurement can analyze the stress situation of GaN crystal. The tensile stress will show a small Raman shift value in the Raman result, while the compressive stress will show a large Raman shift value [9]. The Raman displacement of the pure GaN film without any stress is 567.6 cm^{-1} . While the ST device has an offset of 564.8 cm^{-1} , the SiC on Si device has an offset of 565.2 cm^{-1} , and the Raman displacement of the two test pieces. The peak value of the displacement is small, which means that they are all subjected to tensile stress. Furthermore, ST device has more deviations and bears greater tensile stress. This also causes ST test piece has more defects in buffer layer which affects the reliability of the components. Fig.2 (b) shows XRD measurement results among SiC on Si and ST substrates HEMT.

$$N_{\text{screw}} = \frac{\text{FWHM}_{002}^2}{4.35 * b_{\text{screw}}^2}$$

$$N_{\text{edge}} = \frac{\text{FWHM}_{102}^2}{4.35 * b_{\text{edge}}^2}$$

The dislocation density is made up of N_{screw} and N_{edge} . The lower FWHM value of SiC on Si HEMT shows less dislocation density. The dislocation density of SiC on Si HEMT and ST HEMT is about $4.72 \times 10^9 \text{ cm}^{-2}$ and $1.32 \times 10^{10} \text{ cm}^{-2}$, respectively. SiC on Si HEMT has a similar coefficient of thermal expansion (CTE) and lattice size, so it has fewer traps.

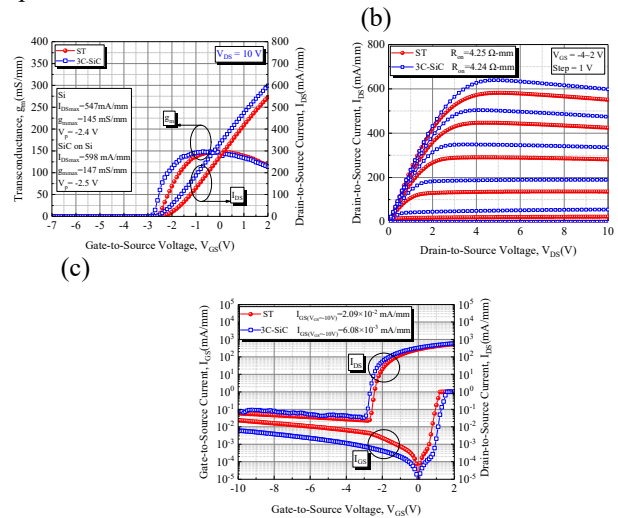


Fig. 3 (a) Measured $I_{DS}-V_{GS}$ at $V_{DS} = 10$ V of the devices, (b) Measured $I_{DS}-V_{DS}$ at V_{GS} from -4 V to 2 V of the devices, (c) Measured $I_{DS}-V_{DS}$ and $I_{GS}-V_{GS}$ characteristic diagram.

Fig.3(a) shows the $I_{DS}-V_{GS}$ characteristic of SiC on Si HEMT and ST HEMT. The $g_{m,max}$ values of SiC on Si HEMT and ST HEMT are 147 mS/mm and 145 mS/mm, respectively. Fig.3(b) shows that the $I_{DS}-V_{DS}$ characteristic of SiC on Si HEMT and ST HEMT. R_{on} values of SiC on Si HEMT and ST HEMT are $4.63 \Omega \cdot \text{mm}$ and $4.77 \Omega \cdot \text{mm}$, respectively. SiC on Si HEMT has better DC characteristics due to the lower lattice mismatch between GaN and SiC. Fig.3(c) SiC on Si and ST HEMT $I_{DS}-V_{DS}$ and $I_{GS}-V_{GS}$ characteristic diagram can analyze the characteristics of Schottky gate. The measurement conditions are $V_{DS}=0$ V, V_{GS} is from -10 V to 2 V, and $V_{GS} = -10$ V is off-state, the gate leakage current I_{GS} of the SiC on Si is 6.08×10^{-3} mA/mm and the gate leakage current I_{GS} of the ST is 2.09×10^{-2} mA/mm. The gate leakage current of SiC on Si HEMT is small than the ST HEMT. Because of growth SiC between GaN buffer and Si substrate to reduce the defects, so the DC measurement has advantage in current, conductivity, Ron and small leakage current than ST HEMT.

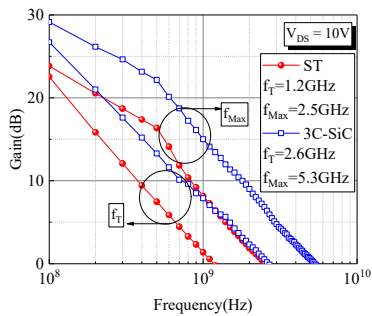


Fig.4 High-frequency of SiC on Si HEMT and ST HEMT.

Fig.4 shows the High frequency characteristic of SiC on Si HEMT and ST HEMT. $V_{DS}=10$ V, $V_{GS}=-1.3$ V, the Current Gain Cutoff Frequency of SiC on Si HEMT and ST HEMT are 2.6 GHz and 1.2 GHz. Maximum Frequency of Oscillation of SiC on Si HEMT and ST HEMT are 5.3 GHz and 2.5 GHz. SiC on Si HEMT has better high-frequency characteristics because SiC can reduce defects between buffer and substrate which is likely to cause signal loss, so it is also helpful for high-frequency.

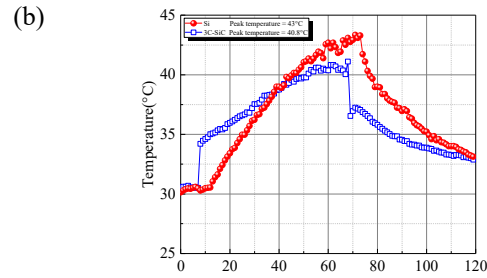
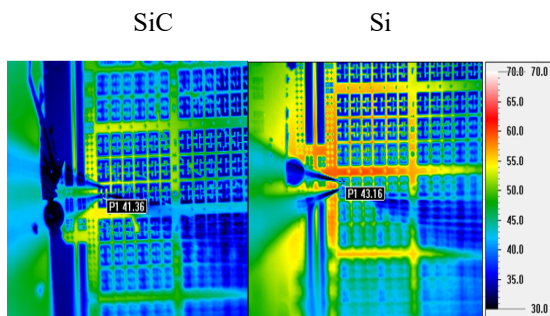


Fig. 5 (a) Surface peak temperature of both HEMTs by infrared thermography, (b) temperature following the time, with the device operating for 60 s.

Fig.5 shows the surface peak temperature of both HEMTs using infrared thermography. They were operating at a current of 60 mA for 60 s. The temperature of SiC on Si HEMT rises quickly at the beginning, but it shows its good thermal expansion coefficient and thermal stability with the increase of time. Surface temperatures were increasing by self-heating, and the peak temperature of the SiC on Si HEMT and ST HEMT was 40.8 °C and 43 °C, respectively. The SiC on Si HEMT having a lower surface peak temperature demonstrates that the SiC substrate can promote the effect of heat dissipation.

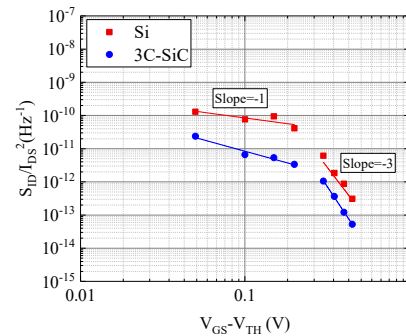


Fig. 6 SiC on Si HEMT and ST HEMT low-frequency noise analysis measurement

Fig.6 shows the low-frequency noise analysis. Through low-frequency noise analysis, the phenomenon of defect capture and release of carriers under different gate bias voltages can be analyzed, and the noise from 10 Hz to 1 kHz can be measured. The signal will decrease accordingly. in Fig. 7, when the frequency is 100 Hz, the gate bias is increased for analysis. The noise change can be clearly seen when the device is operating in the on state. Therefore, the gate bias will change from V_p which starts to increase. With the increase of V_{GS} , the noise also has a downward trend, and there are two slopes of V_{GS}^{-1} and V_{GS}^{-3} . V_{GS}^{-1} is mainly the

noise near the channel layer, while V_{GS}^{-3} is mainly the buffer layer. Therefore, it can be seen that under V_{GS}^{-3} , the noise of SiC on Si HEMT is lower, which means that the defect density of SiC on Si HEMT is less, and the defects capture and release carriers less, and also the results of Raman measurements can be verified.

CONCLUSIONS

A conventional HEMT growth SiC between GaN buffer and Si substrate which is used in this work. The device exhibits better DC characteristic, high-frequency and SiC on Si HEMT also have low leakage current than conventional HEMT. SiC has a higher thermal conductivity. Therefore, GaN HEMTs grown on a SiC substrate improve the lattice mismatch and the reliability of the temperature. We can know from the thermal image measurement that due to the good thermal stability and thermal conductivity of the SiC on Si HEMT, the heat dissipation is also better than the ST HEMT. Due to use SiC between GaN and Si, we can reduce lattice mismatch which leads to defects. The SiC on Si HEMT can reduce defects emerge noise which we can see in the low-frequency noise analysis Measurement. Because of SiC is expensive, we may pay more money on this wafer. In the future, we can attempt growth SiC on Si to reduce Buffer and substrate defects and then effectively reduce costs to improve the characteristic of device.

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