Advanced MOCVD Technology for RF-HEMT Growth on SEMI-Standard Large-Area (111) Silicon Substrates

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High electron mobility transistors (HEMT) based on the group III-nitride semiconductor family are well suited to meet the requirements of the 5G and 6G telecommunication standards [1,2]. Mass production of such device stacks is particularly advantageous using Metal Organic Chemical Vapor Deposition (MOCVD) on SEMI-standard large-area (150 or 200 mm diameter) Si wafers due to their low cost, availability and compatibility to existing CMOS process lines.

However, several challenges exist for MOCVD of RF-HEMT stacks on large-area silicon substrates. The large lattice and thermal expansion mismatch of GaN and AlN to Si combined with the relatively low thickness, weak doping and thus low stiffness of the Si substrate pose several constraints in terms of wafer bow management and temperature uniformity [3]. Also, for low-loss operation of transistors at high frequencies, parasitic conductivity in the substrate must be avoided which means that diffusion of Al and Ga during heat-up and epitaxy is to be minimized [4,5].

Thin Si wafers typically show a concave bowing during heatup and initial growth steps which leads to a strongly convex temperature profile. This can lead to slip line formation and even plastic wafer deformation. To avoid this, the AIXTRON G5+ C Planetary® MOCVD batch reactor (for 5×200 mm or 8×150 mm) is now also equipped with Ar gas for the gas foil rotation® (GFR®) of the wafer carriers (satellites). Due to the lower thermal conductivity of Ar compared to H_2, the temperature in the center part of the satellite is reduced while the edge is mostly unchanged due to in-diffused H_2 from the carrier gas. This can compensate a large part of the bow-induced temperature gradient preventing slip line formation. In Fig. 1, optical microscopy images of 675 µm thick, high-resistive 150 mm Si wafers which have been heated to 1050 °C for 10 min without further growth are displayed. While standard H_2 GFR gas produces distinct slip lines as visible in Fig. 1 a, the usage of Ar GFR gas leads to a featureless surface as shown in Fig. 1 b. The option to switch between Ar, N_2 and H_2 GFR gas also allows to keep a smooth temperature profile in further growth steps.

The subsequent growth of a baseline RF-HEMT stack on SEMI-standard high-resistivity (R > 3 kΩ·cm) 725 µm 200 mm (111) Si was initiated with an AlN nucleation layer, followed by a C-doped AlGaN and GaN buffer and a 250 nm thick GaN channel.

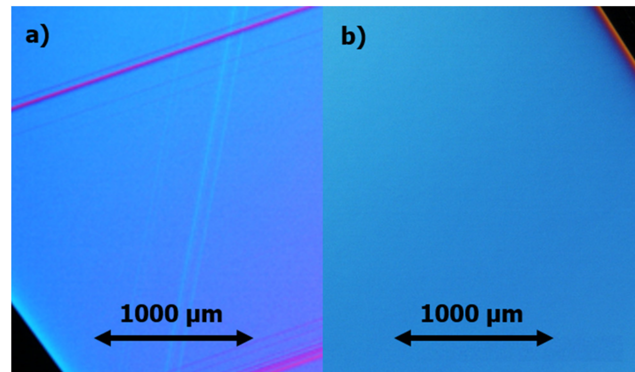

Fig. 1 Optical microscopy images of 675 µm thick (111) Si wafers after 10 min heat cycle at 1050°C using either H_2 (a) or Ar (b) rotation gas below satellite.

On top, a 1 nm AlN interlayer and a 10 nm AlInN barrier was added without any capping layers. In one sample, a 200 nm AlGaN back-barrier with an Al content of 5% was added below the GaN channel to compare a double heterostructure (DH-) to a single heterostructure (SH-) HEMT.

a)

Layer	Thickness
$Al_{0.82}In_{0.18}N$ barrier	10 nm
AlN spacer	1 nm
GaN channel	250 nm
GaN:C ~1E19 cm^{-3}	1.5 µm
$Al_{0.20}Ga_{0.80}N$:C ~5E18 cm^{-3}	180 nm
AlN	140 nm
High-resistivity Si (111)	725 µm

b)

Layer	Thickness
$Al_{0.82}In_{0.18}N$ barrier	10 nm
AlN spacer	1 nm
GaN channel	250 nm
$Al_{0.05}Ga_{0.95}N$ back-barrier	200 nm
GaN:C ~1E19 cm^{-3}	1.5 µm
$Al_{0.20}Ga_{0.80}N$:C ~5E18 cm^{-3}	180 nm
AlN	140 nm
High-resistivity Si (111)	725 µm

Fig. 2 Investigated a) SH- and b) DH-HEMT layer stacks.

Both SH- and DH-HEMT stacks are shown in Fig. 2 a and b, respectively. C-doping of ~ $5 \cdot 10^{18}$ - $1 \cdot 10^{19}$ cm^{-3} is achieved by additional introduction of gaseous C_2H_4 during GaN and AlGaN growth. Distributing C_2H_4 in two injection levels leads to uniform C doping with center-to-edge variation < 20%. Both SH- and DH-HEMT stacks show an almost identical sheet resistance of ~ 220 Ohm/sq. with an on-wafer 1 σ of ~ 1.5% as measured by the eddy current technique. This is confirmed by Hall measurements showing a sheet electron density n_s of ~ $1.9 \cdot 10^{13}$ cm^{-2} and a mobility μ_n of ~ 1,500 cm²/(V·s).

A challenge for uniform growth on SEMI-standard Si wafers is their low thickness of 675 µm and 725 µm for 150 mm and 200 mm diameter, respectively. Conventional satellites in the G5+ C MOCVD tool have been designed with a recess depth of 1.4 mm to accommodate thicker wafers also. For thin wafers, this leads to a significant step creating lower local concentration of group III species and thus reduced growth at the wafer edge. To avoid this, a new design with modified recess depth was established matching the Si substrate thickness. The resulting total thickness profiles for standard and matched recess are compared (for the SH-HEMT) in Fig. 3. The 1σ standard deviation is largely reduced from 1.9% to 0.5%. Note that the composition uniformity of ternary layers is not affected by this change. Using both new technologies, good on-wafer and wafer-to wafer thickness uniformities with 1σ < 1% for all layers are achieved, without edge cracking or slip lines and a final wafer bow < 50 µm.

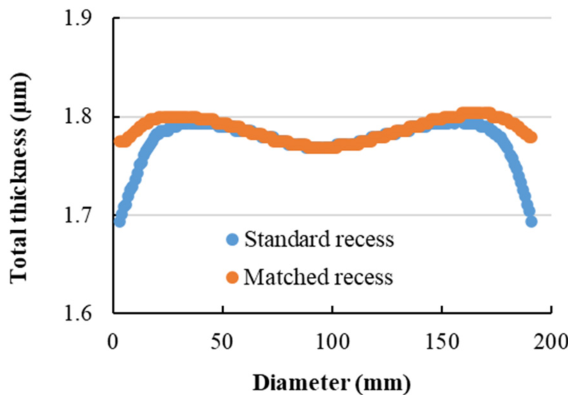

Fig. 3 Thickness profiles for SH-HEMT stacks on 200 mm Si using standard and recess-matched satellites.

The challenge related to parasitic dopant diffusion for GaN-on-Si is addressed on the one hand by ensuring a high cleanliness of the reactor hardware. We demonstrate that our established Cl_2 *in situ* cleaning procedure efficiently removes Al and Ga residuals before the next growth process is initiated. This is verified by spreading resistance profiling (SRP) on the high-resistive Si substrates heated up to a temperature of 1050°C for 10 min which shows no increase of conductivity at the wafer surface as shown in Fig. 4.

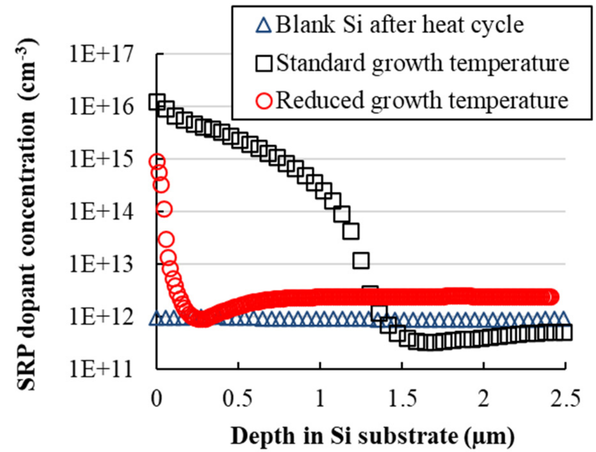

Fig. 4 Dopant concentration in Si substrate for blank Si after heat cycle and for 2 µm thick AlN/AlGaN/GaN layer stacks using different growth temperatures. All experiments are performed in an *in situ* cleaned reactor chamber.

On the other hand, parasitic diffusion during epitaxy is minimized by reduced growth temperatures and further process tuning. The standard, high-temperature process is producing a diffusion tail with a depth of ~ 1.5 µm, visible both in a secondary ion mass spectroscopy (SIMS) profile for Al (not shown) and the SRP dopant profile which is displayed in Fig. 4 also. After optimization of the growth process towards lower temperatures, this tail in SRP is reduced to a depth of less than 0.3 µm.

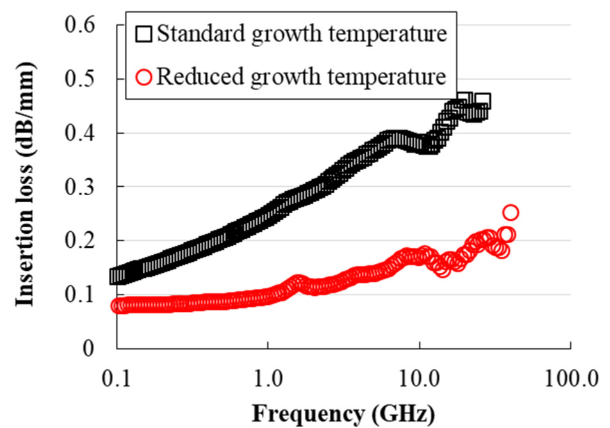

Fig. 5 RF insertion loss measured on AlN/AlGaN/GaN layer stacks for standard and reduced growth temperatures.

As a result, the insertion loss in a coplanar waveguide (CPW) test configuration (lines of 3 mm length, 120 µm width and 60 µm separation) on layer stacks without barrier shows a clear reduction from ~ 0.45 dB/mm to <0.3 dB/mm at 28 GHz (illustrated in Fig. 5). RF-transistor test structures with a simple trapezoidal gate structure and gate lengths L_g = 100 - 150 nm have been fabricated by e-beam lithography on 150 mm Si wafers using the SH-HEMT stack shown in Fig. 2 a. High output current densities of 1.75 A/mm at V_{ds} = 3.3 V and a peak transconductance $g_{m,max}$ of ~ 470 mS/mm are obtained for 150 nm gates. Small-signal transistor measurements show a maximum transit and maximum oscillation frequency f_t and f_{max} of ~ 85.5 and 68.5 GHz, respectively, for devices with L_g = 100 nm, mainly limited by the non-optimized transistor layout, gate resistance and short-channel effects.

Furthermore, a full device lot on 200 mm Si with 725 um thickness has been introduced into the imec pilot line with gate lengths L_g down to 130 nm. The bow has remained very well below the line specifications throughout the lot processing. No wafer breakage occurred. In the following, the device dimensions are L_g = 130 nm, L_{sg} = 1.5 µm, L_{gd} = 1.75 µm and L_{fp} = 0.5 µm.

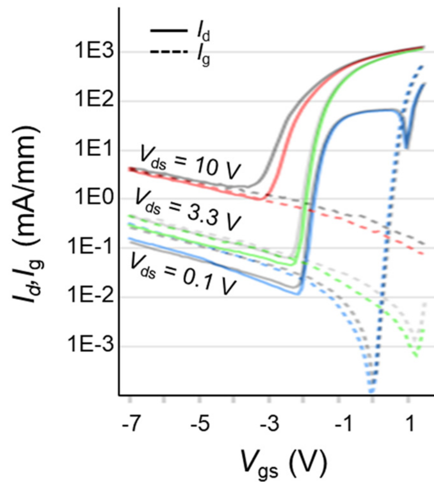

Fig. 6 Semi-logarithmic transfer characteristics and gate leakage current for SH-HEMT (grayscale) and DH-HEMT (colored). L_g is 130 nm. All values are median values of 21 dies across the 200 mm wafer.

Median values of semi-logarithmic transfer curves and gate leakage current are shown for the SH-HEMT and DH-HEMT in Fig. 6. The introduction of the back-barrier leads only to a small reduction of drain leakage current at low bias. At high bias however – when lateral electric fields are larger – the back-barrier clearly proves efficient for reducing short-channel effects such as drain-induced barrier lowering (DIBL) and degraded sub-threshold swing (SS). Gate leakage currents are slightly lower for the DH-HEMT. The AlInN barrier devices show a DC performance that is in line with typical devices reported in literature [6,7]. From the linear plot, transconductance values have been extracted at V_{ds} = 3.3 V. Devices with this back-barrier show a slightly improved average peak transconductance g_m of 540 mS/mm versus 517 mS/mm for the reference stack.

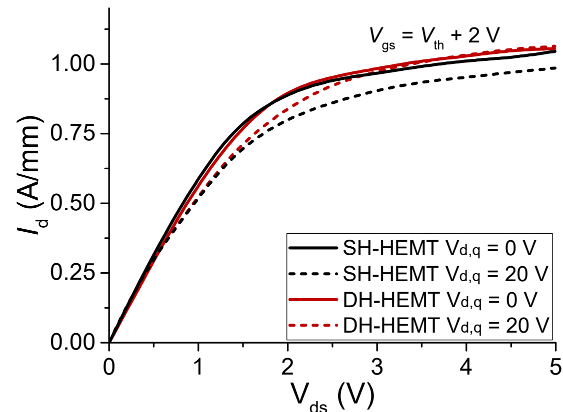

Fig. 7 Double-pulsed output characteristics for SH-HEMT (black) and DH-HEMT (red) for $V_{d,q}$ = 0V (solid) and $V_{d,q}$ = 20 V (dashed). $V_{g,q}$ = V_{th} – 2.5 V.

To assess the dynamic performance of the devices, double-pulsed I-V measurements have been performed with a pulse width of 250 ns and a duty cycle of 0.1%. Output characteristics for zero and 20 V quiescent drain bias $V_{d,q}$ are shown in Fig. 7. V_{gs} was fixed at V_{th} +2 V. For both SH-HEMT and DH-HEMT a slight knee walk-out is visible. This effect is smaller for the DH-HEMT, indicating reduced trapping due to screening of the C impurities by the AlGaN back-barrier. A penalty of about 0.3 V must be considered. For a 28 V device, that would account to about 1.2% reduction in voltage swing along the load line. In case of the SH-HEMT, one has to bear with 8% reduction in $I_{d,max}$ or 1.5 V (6%).

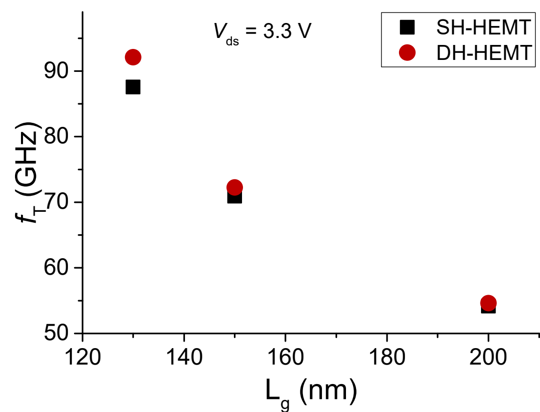

Fig. 8 Extracted values for cut-off frequencies f_T vs. gate length L_g for the SH-HEMT (black dots) and DH-HEMT (red circles) at V_{ds} = 3.3 V and V_{gs} @ $g_{m,max}$.

Small-signal parameters have been measured for devices with dimensions as indicated before. Devices with L_g of 130 nm,

150 nm and 200 nm have been assessed and the data is shown in Fig. 8. f_T of 54 GHz was obtained for the devices with L_g = 200 nm for both SH- and DH-HEMT. At L_g = 130 nm, f_T increases to 87.6 GHz for the SH-HEMT and 92.1 GHz for the DH-HEMT, giving a very good $f_T \times L_g$ product of 12.0 GHz·µm. It is expected that further refinement of the epitaxial layer stack, e.g., by improving electrostatic control through a thinner GaN channel, will give a boost in ON/OFF ratio, sub-threshold swing, dynamic performance and f_T at scaled gate lengths.

Conclusions

We have presented modifications of the reactor setup to optimize the MOCVD technology for group III-nitride epitaxy on SEMI-standard. thickness Si substrates. Argon GFR® has been used to eliminate slip lines and cracks in the Si substrate. Satellites with a recess matched to the SEMI-standard thickness results in largely improved thickness uniformities. *In situ* cleaning with Cl_2 prevents any contamination of the Si substrate during the desorption step. Together with a reduction of the thermal budget of the epitaxial runs, this results in low buffer insertion losses. Test devices have been successfully fabricated and characterized to show their suitability for RF amplifiers. 200 mm wafers have finally been processed in the imec pilot line with very good bow control and without wafer breakage. Both SH- and DH-HEMT show a performance well comparable to state-of-the-art devices in literature. A significant performance improvement can be found for the DH-HEMT devices for lowest gate lengths of 130 nm.

Acknowledgments

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Acronyms

HEMT: High Electron Mobility Transistor
MOCVD: Metal Organic Chemical Vapor Deposition
GFR: Gas foil rotation ®
SH: Single Heterostructure
DH: Double Heterostructure
SIMS: Secondary Ion Mass Spectroscopy
SRP: Spreading Resistance Profiling
CPW: Coplanar Waveguide
DIBL: Drain-Induced Barrier Lowering
SS: Sub-threshold Swing