3.4 – 3.8 GHz 20W Compact 2-stage GaN HEMT Power Amplifier using IPDs on HPSI SiC substrates

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Abstract

In this report, compact 2-stage PAs (Power Amplifiers) have been designed and fabricated with GaN HEMT discrete devices and IPDs (Integrated Passive Devices) on SiC substrate. 0.7- and 3.5-mm total gate periphery GaN HEMT devices on SiC substrate were fabricated by Wavice foundry process with 0.3 um gate length. The IPDs include MIM capacitors with SiNx insulator, spiral inductors with 5 um thick electro-plated Au metal lines, TaN resistors and through-substrate vias (TSVs). 2-stage PAs were assembled on an 8 x 8 mm^2 area and showed over 20 W peak power output, 23.3 dB power gain, and over 38 % PAE for the 3.4 ~ 3.8 GHz frequency band.

INTRODUCTION

GaN HEMT (high electron mobility transistor) has been widely adopted for 5G base stations, high power radar systems, electronic warfare systems because of the superior performance of the technology such as high output power density, high breakdown voltage, high thermal conductivity, high frequency operations etc. [1] To support the requirements of a wider range of high frequency applications, the HPAs need to have high output power, high efficiency, and small form factor with lower manufacturing cost. [2]

The quasi-MMICs fabricated by hybrid integration of low cost IPDs and high-power transistors are one of the most promising technologies for the next generation telecommunication systems. [3] The other solutions such as hybrid HPAs on a printed circuit board (PCB) or monolithic microwave integrated circuits (MMICs) are either too bulky or too costly.

Small footprint IPDs have been developed on high resistivity silicon (HRS), high purity semi-insulating (HPSI) SiC, glass, semi-insulating GaAs substrates or as a form of low temperature co-fired ceramic (LTCC). [4] Performancewise, all the above technologies are feasible for high frequency applications. However, in terms of manufacturing cost and mass production capability, HRS, HPSI SiC and Glass substrates are better than LTCC or GaAs. [5-8] Also for high power applications, HPSI SiC is a more feasible candidate than HRS, glass or GaAs substrates because of the superior thermal conductivity of SiC wafers. [9-13]

IPDs on HRS have been demonstrated with or without TSV. [14, 15] and are available through an open foundry. [16,17] To reduce the RF transmission loss, higher resistivity of the substrate is desirable. Also, to further reduce the footprint of HPAs, it is essential to have a TSV process to connect the circuit components on the front side of the substrate to the back side metal.

In this work, IPDs on HPSI SiC substrates with TSV process have been demonstrated. The compact 2-stage HPAs have been designed and assembled using the IPDs and GaN HEMT devices on a Cu heat sink with 8 x 8 mm^2 area.

DESIGN AND FABRICATION OF POWER AMPLIFIERS

1) PA design

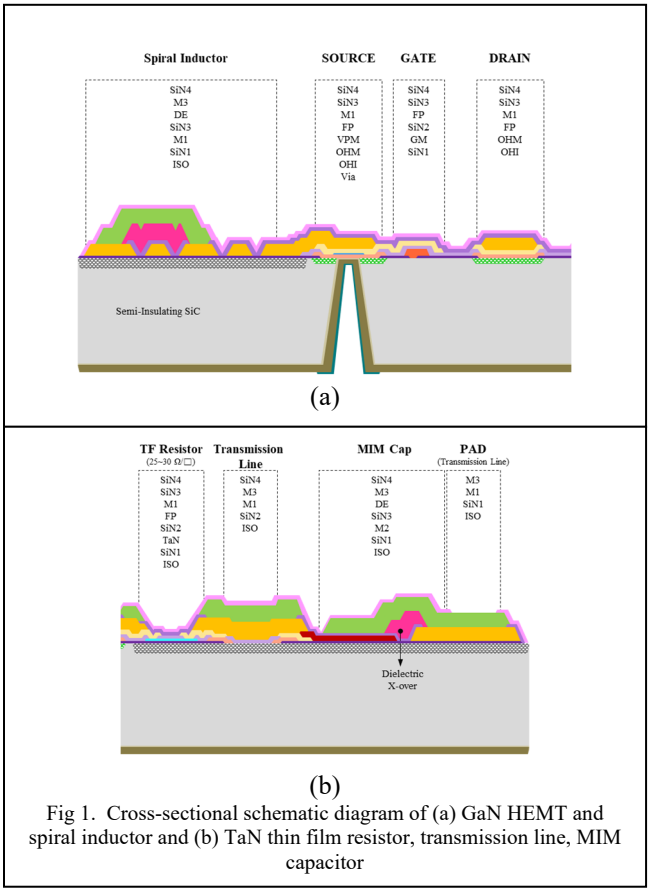


Fig 1. Cross-sectional schematic diagram of (a) GaN HEMT and spiral inductor and (b) TaN thin film resistor, transmission line, MIM capacitor

Figure 1 (a) shows GaN transistor and inductor, (b) shows resistor, MIM capacitor and transmission line. Table 1 shows the definition and the dimension of each layer described in Figure 1.

TABLE I
LAYER INFORMATION FROM FIGURE 1.

Color	Symbol	Layer	Thickness (nm)
	DE	Dielectric	>8um
	OHM	Ohmic Metal	260
	GM	Gate Metal	600
	FP	Field Plate Metal	800
	M1	Metal 1	5000
	M2	Metal 2	2000
	M3	Metal 3	5000
	TFR	Thin Film Resistor (TaN)	90
	VPM	Via Protection Metal	300
	BM1	Backside Metal 1	600
	BM2	Backside Metal 2	7000
	OHI	Ohmic Ion Implant	-
	ISO	Isolation Implant	-
	SiN1	SiN1 Passivation	120
	SiN2	SiN2 Passivation	250
	SiN3	SiN3 Passivation	500
	SiN4	SiN4 Passivation	250

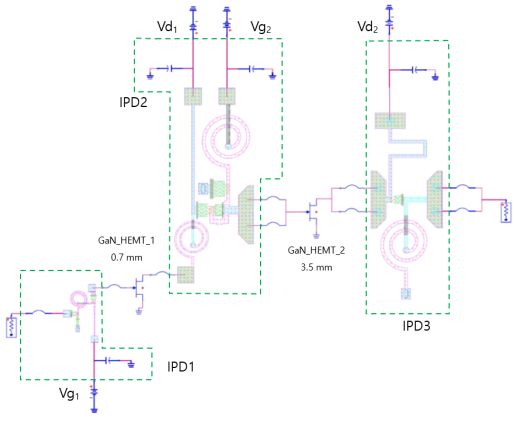
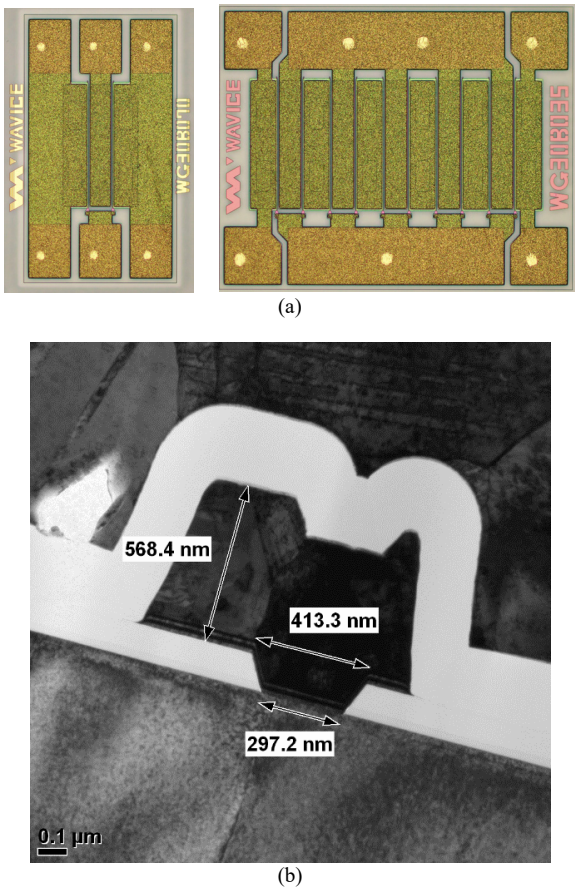


Fig. 2. 2-stage PA design with 2 GaN HEMT devices and 3 pieces of IPDs designed in ADS environment

The device models of GaN HEMT transistors and passive devices are available for Keysight ADS and Cadence Microwave Office circuit design software. Figure 2 shows the schematic diagram of the PA circuit in ADS environment.

2) Fabrication Process – The device fabrication process is composed of GaN HEMT transistor and IPD device fabrication. The fabrication process of GaN HEMT MMIC of Wavice comprises implanted and recess-etched ohmics, stepper-defined 0.3 um gates, electro-plated source-connected field plates (SCFPs), electro-plated 5 um thick metal layers, TaN thin film resistors, through-SiC vias, 85 um SiC substrate after thinning, 7 um thick back side metal. [18] Figure 3 shows (a) the optical microscope images of 0.7- and 3.5-mm gate periphery devices and (b) a SEM cross-section of the gate area.



(a)

(b)

Fig. 3. (a) optical microscope pictures of 0.7 mm (Left) and 3.5 mm (Right) gate periphery devices and (b) the SEM cross section of gate area showing 0.3 um at the foot of the gate

The IPD process consists of TaN resistors with 25 Ω/□ sheet resistivity, SiNx based MIM capacitors with 7.7 pF/mm^2 capacitance density, 2 layers of 5 um thick interconnect metals, spiral inductors with dielectric cross over. An identical IPD process on HRS substrates in Wavice was reported elsewhere. [19] Figure 4 shows the optical microscope images of fabricated passive devices. The process is based on 4" HPSI SiC wafers. MMICs are processed on GaN epi on SiC wafers while for IPDs the process was done on bare HPSI SiC wafers without GaN epi. For both cases, the substrates were thinned to 85 um thickness and electro-plated 7 um thick metal is coated on the backside of the wafer after TSV etch.

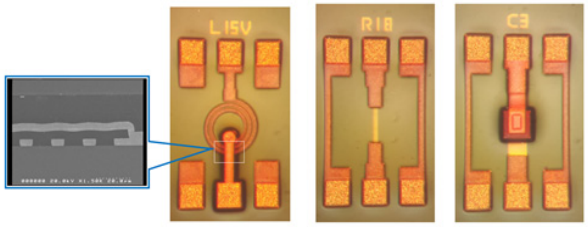


Fig. 4. From the left, cross sectional SEM image of spiral inductor, microscope images of spiral inductor, TaN resistor, and MIM capacitor

3) Assembly process – The GaN HEMT devices and 3 IPDs were bonded to an 8 x 8 mm^2 Au-plated copper heat sink using Ag epoxy. After the wafer bonding, Au wires were ball-bonded to electrically connect the devices. Figure 5 shows the 2-stage PA after assembly is completed. The copper heat sink with assembled PAs was inserted in a test fixture and the pads were wire bonded for further testing.

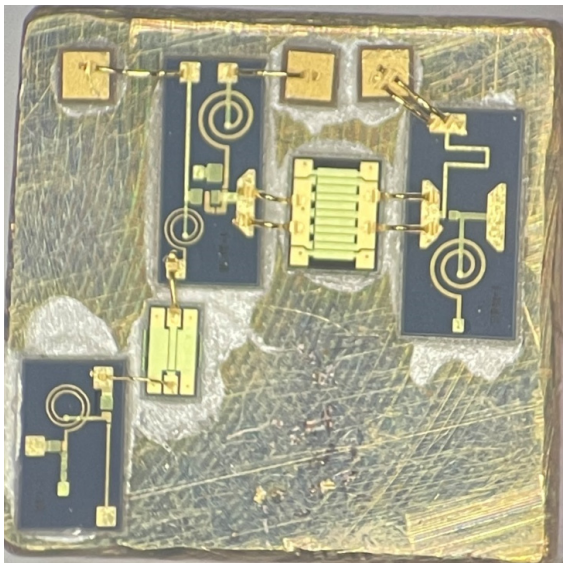
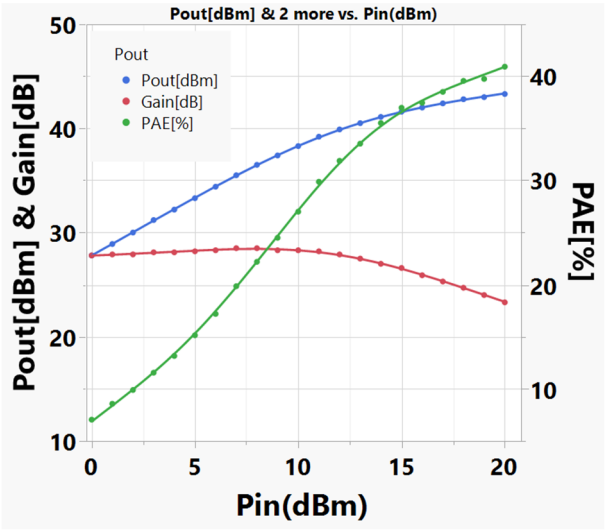


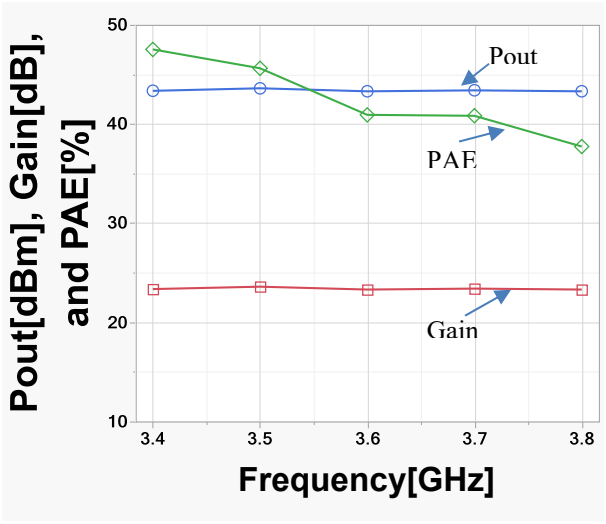
Fig. 5. Optical microscope picture of a 2-stage PA assembled on an 8 x 8 mm^2 Cu heat sink.

Results and Discussions

Figure 6 shows the RF performance of the 2-stage PAs. The PAs were biased at Class AB condition and the drain voltage was 50 V. The RF pulse was 100 us wide with 10% duty cycle. The measurement was done at room temperature without active cooling. Figure 6 (a) shows a power sweep data at 3.6 GHz. 23.3 dB power gain, over 20 W output power, and over 38 % PAE were measured for the 3.4 ~ 3.8 GHz frequency range as shown in figure 6 (b).



(a)



(b)

Fig. 6. (a) power sweep data at 3.6 GHz. (b) Gain, Pout and PAE for 3.4 – 3.8 GHz frequency range at Pin = 20 dBm. The measurement was done with Vd=50V, Pulse width=100 usec, duty cycle=10% and Class AB.

Conclusions

A compact hybrid packaged 2-stage GaN HEMT quasi-MMIC style PA has been demonstrated with IPDs on HPSI SiC substrates for the first time. The PA was assembled on an 8 x 8 mm^2 copper heat sink with 2 GaN HEMTs with 0.3 um gate length and 3 pieces of IPD circuits. Over 20 W output power, 23.3 dB power gain and over 38% PAE were measured

at the 3.4~3.8 GHz band with 50 V drain bias and 100 usec, 10 % duty cycle RF pulse input. To the best of author's knowledge, this is the highest peak power from hybrid packaged 2-stage GaN PAs reported so far for the frequency range. Further improvement in IPD design, wafer level packaging, reliability testing is in progress.

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ACRONYMS

HEMT: High Electron Mobility Transistor
HPSI: High Purity Semi Insulating
IPD: Integrated Passive Device
LTCC: Low Temperature Cofired Ceramic
HRS: High Resistive Silicon
TSV: Through Substrate Via
MIM: Metal Insulator Metal
MMIC: Monolithic Microwave Integrated Circuit
ADS: Advanced Design System
PCB: Printed Circuit Board
PAE: Power Added Efficiency
RF: Radio Frequency
PA: Power Amplifier
HPA: High-Power Amplifier