100-V GaN HEMT Technology with Record-High Efficiency at C-Band Frequencies

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Abstract

We report on a 100-V GaN HEMT technology targeting applications through X-band. A revised epitaxial structure as well as changes in the intrinsic device features lead to substantial improvements in efficiency and reduction in output capacitance, when compared to a previous process version. Load pull measurements at 2.0 GHz reveal a PAE in excess of 84 % while the maximum power density is more than 15 W/mm. Even at 7.2 GHz, the devices demonstrate exceptionally high PAE of more than 66 % and a power density of 13.8 W/mm. To the best of the authors' knowledge, both efficiency values set records at their respective frequencies for 100-V GaN HEMTs.

Introduction

The growing demand for efficiency improvement in very-high-power applications also drives the development of solid-state technologies capable of delivering kilowatt-level output powers. Although vacuum tube technology is still dominating the market for most of these applications, the major drawbacks, such as high-voltage supply, sudden device failure and low phase stability, make many system operators turn to solid-state powered solutions. In particular, continuous-wave (CW) applications make high efficiency an essential requirement for long-term reliable operation.
This paper focusses on process enhancements of our 100-V AlGaN/GaN high electron mobility transistor (HEMT) technology resulting in substantial improvements in terms of achievable device efficiency as well as operating frequency.

Technology and Fabrication

Epitaxial growth is performed by metal-organic chemical vapor deposition (MOCVD) on 4-inch semi-insulating SiC substrates. A GaN buffer layer is grown on top of an AlN nucleation layer followed by a 25 nm thick barrier layer of $Al_{20}Ga_{80}N$ and 3 nm of undoped GaN.
A gate length of 0.50 µm was chosen in order to improve control of the electrical field underneath and next to the gate edge. All devices feature a source-terminated field plate (STFP) to further shape the electrical field and optimize the feedback capacitance, which is crucial to achieve high gain. In order to reduce the source inductance, individual through-wafer via holes are placed inside the source regions.

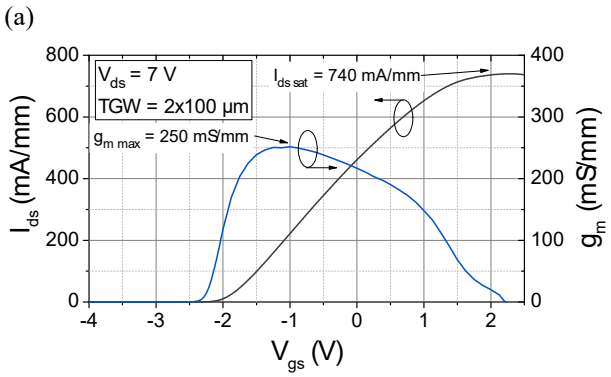
DC Performance

An essential requirement to achieve high performance at an elevated supply voltage of 100 V is to maintain adequate charge control. In order to ensure that, close attention to the electrostatic properties of the devices has to be paid to avoid pronounced short-channel effects. One measure is to choose a high ratio of gate length and gate-to-channel distance, which is greater than 17 in our case. Additionally, employing a rather thick AlGaN barrier layer with moderate Al mole fraction ensures relaxed electrical field strength conditions in the channel, further suppressing short-channel effects.
The high supply voltage also poses difficulties when trying to achieve good device efficiency. Highly efficient amplifier modes require dynamic voltage waveforms exhibiting peak values of more than 3.5 times the supply voltage [1]. Therefore, the devices need to provide sufficiently high voltage robustness. To accomplish that, the spacing between the gate and drain electrodes has to be enlarged, hence, also the device's on-resistance (R_{on}) increases. However, this contradicts the aim of obtaining high efficiency. Thus, the design of the intrinsic device features plays a major role in the overall device performance. An overview over the DC characteristics of the technology is given in Table I.

TABLE I
DC Characteristics of Fraunhofer IAF
100-V GaN HEMT Technology

Maximum Transconductance @ V_{ds} = 7 V	250 mS/mm
Maximum Drain Current @ V_{ds} = 7 V	740 mA/mm
Gate-Drain Breakdown Voltage	> 350 V
Threshold Voltage	-2.3 V
On-Resistance	4.2 Ω·mm
Drain-Induced Barrier Lowering	< 1 mV/V

DC transfer curves for a 2x100 µm total gate width (TGW) device have been measured on-wafer at a drain-source voltage (V_{ds}) of 7 V, as shown in Fig. 1. (a). The maximum transconductance ($g_{m\ max}$) and saturated drain current ($I_{ds\ sat}$) are 250 mS/mm and 740 mA/mm, respectively. The threshold voltage (V_{th}), when extracted at a drain-source current (I_{ds}) of 0.1 mA/mm, is -2.3 V. Since the nominal supply voltage of the technology is more than an order of magnitude higher than the rather low V_{ds} that was chosen for recording the transfer



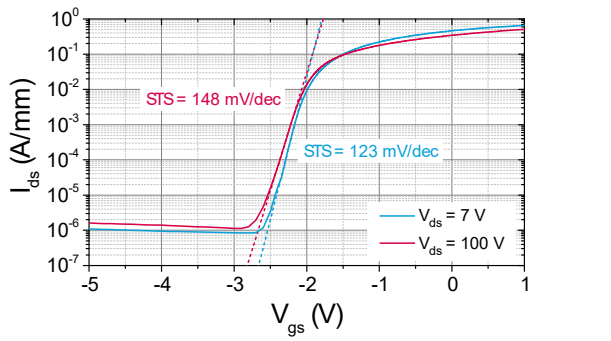


Fig. 1. (a) Measured DC transfer characteristics of a 2x100 µm device at V_{ds} = 7 V and (b) superimposed logarithmic data of I_{ds} vs. V_{gs} at a V_{ds} of 7 V and 100 V, respectively.

characteristics, we repeated the measurement for the same device at V_{ds} = 100 V. The comparison of both measurement results lets us examine short-channel effects present in the devices. The superimposed data of I_{ds} in logarithmic representation for both measurements, at a V_{ds} of 7 V and 100 V, respectively, is shown in Fig 1. (b).

The logarithmic scale allows to easily extract the respective subthreshold slopes (STS) for both V_{ds} values. The analysis yields a low value of 123 mV/decade at 7 V, proving good charge control of the gate. Raising V_{ds} to 100 V only slightly affects the STS, which shows a 20 % increase towards 148 mV/decade. Furthermore, by comparing V_{th} at both V_{ds} values we can quantify drain-induced barrier lowering (DIBL). As stated before, V_{th} at V_{ds} = 7 V is -2.3 V. When extracting V_{th} at a supply voltage of 100 V, a slightly negative shift by 80 mV can be observed, yielding a value of -2.38 V. Since the difference in V_{ds} between the two measurements amounts to 93 V, an ultra-low DIBL of less than 1 mV/V is obtained, demonstrating the impeccable electrostatic properties of the devices. This also becomes clear from the only minor change in drain leakage current, which increases by a factor of two. The different evolution of I_{ds} in the on-state can be attributed to thermal effects, since at 100 V the device dissipates 11 W/mm during the on-wafer measurement. As previously stated, the breakdown voltage (V_{br}) needs to be significantly higher than the targeted supply voltage of the

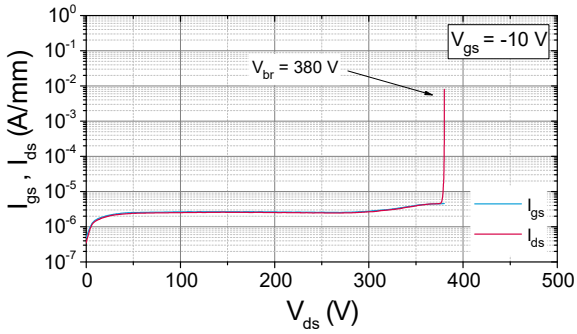


Fig. 2. Drain-source breakdown measurement of a 6x200 µm device.

devices, since under RF drive voltage peaks at the intrinsic current generator plane can reach up to a factor of 3.5 of the supply voltage, e.g. when operated in class-E [2]. Fig. 2. shows the drain-source breakdown characteristics of a 6x200 µm device with the gate-source voltage (V_{gs}) biased in deep pinch-off at -10 V. V_{br} reaches an impressive value of 380 V, leaving enough headroom for dynamic voltage peaking.

Pulsed DC-IV curves, measured for a 6x400 µm device, are given in Fig. 3. The output characteristics have been measured for three different quiescent bias conditions:

- Zero bias (V_{Qgs} = 0 V, V_{Qds} = 0 V)
- Cold pinch-off (V_{Qgs} = -5 V, V_{Qds} = 0 V)
- Hot pinch-off (V_{Qgs} = -5 V, V_{Qds} = 100 V).

A pulse width of 4 µs and a duty cycle of 1 % were chosen. For the ease of presentation only data for a pulsed V_{gs} of +2 V are shown, which is close to where $I_{ds\,sat}$ is reached. Extracting R_{on} and the knee voltage (V_k) from the zero bias condition, we obtain a R_{on} of 4.2 Ω·mm and a V_k of approximately 5.0 V. Compared to commercial 50-V GaN technologies, even quite recently introduced ones, the achieved R_{on} is only around 30 % higher [3].

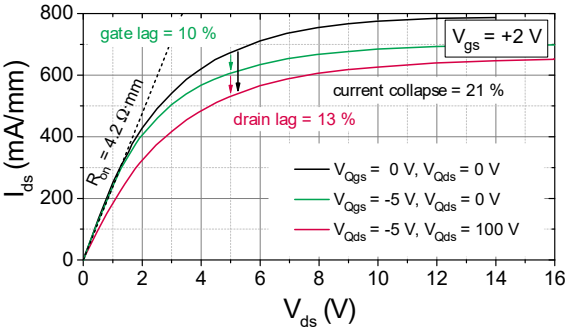


Fig. 3. Pulsed DC-IV data with a pulse width of 4 µs and a duty cycle of 1 % of a 6x400 µm device. Only data for a pulsed V_{gs} of +2 V is shown, which is close to where $I_{ds\,sat}$ is reached

When looking at the cold and hot pinch-off curves, we can observe a slight knee walkout. Still, gate and drain lag are rather low at 10 % and 13 %, respectively, especially when considering the high static V_{ds} of 100 V during the hot pinch-off measurement. In total, the current collapse amounts to 21 %. Further improvements of the surface passivation as well as buffer recipe could most certainly suppress lagging phenomena even more. In particular, load impedances yielding high output power density (P_{out}) would benefit from that since both, the maximum P_{out} and efficiency at maximum $P_{out,}$ heavily depend on the dynamic I_{ds} as well as V_k.

RF Performance

Operating devices in class-AB mode does not yield the maximum achievable efficiency, since the maximum drain efficiency (DE) for that type of operation is limited to 78.5 %. By applying harmonic termination, it is theoretically possible to reach a DE of 100 %. To maintain the capability to effectively tune harmonic impedances also at higher frequencies the output capacitance (C_{out}) has to be kept as small as possible.

By careful tuning of the STFP extension in combination with the thicknesses of the passivation layers, we could achieve a low C_{out} of 0.24 pF/mm, yet maintaining strong control over the electrical field close to the gate. This corresponds to a 40 % reduction in C_{out} when compared to our previous process [4]. In addition, when benchmarking this value against other 100-V GaN technologies, it is more than a factor of two smaller [5].

This also translates to excellent large-signal performance as can be seen from the load pull results at 2.0 GHz and 7.2 GHz, given in Fig. 4. and Fig. 5., respectively. Measurements at 2.0 GHz were performed on a device with a gate periphery of 6x400 µm under pulsed conditions (100 µs pulse width, 10 % duty cycle). To improve the thermal behavior, the dies were attached to CPC141 carriers with a silver sinter paste.

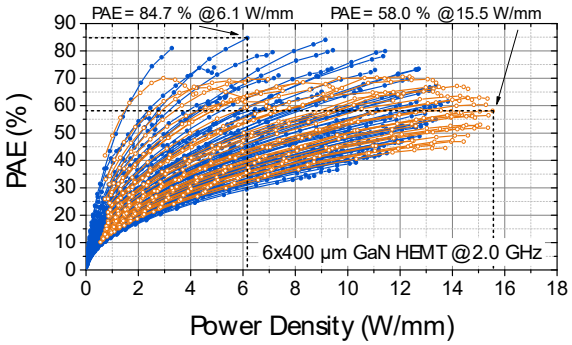


Fig. 4. Fundamental (orange) and harmonic (blue) load pull results of a 6x400 µm device, when measured up to a G_T compression of 3 dB at 2.0 GHz. The bias was set to V_{ds} = 100 V, I_{ds} = 5 mA/mm.

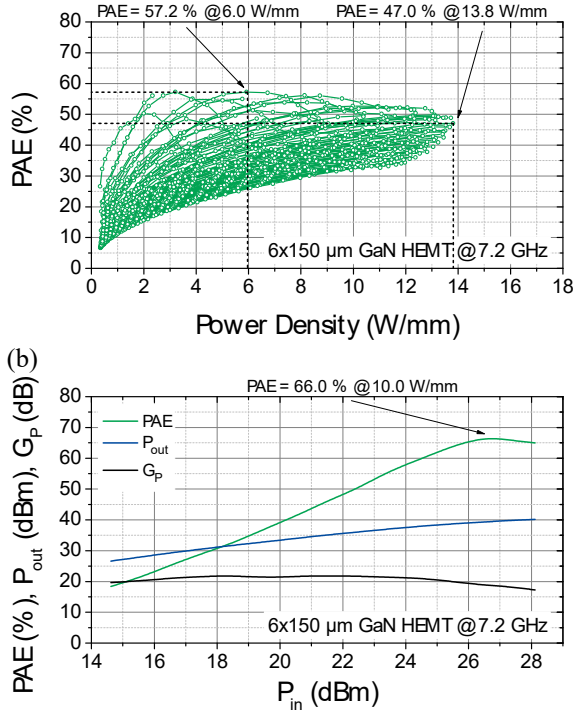


Fig. 5. (a) Fundamental load pull results of a 6x150 µm device, when measured up to a G_T compression of 3 dB at 7.2 GHz. The bias was set to V_{ds} = 100 V, I_{ds} = 5 mA/mm.
(b) Power sweep of the same device for a trade-off load impedance with additional second harmonic impedance tuning at the output, optimized for maximum PAE.

Results are given for both fundamental tuning only and fundamental tuning with second harmonic impedances at in- and output set for optimal power-added efficiency (PAE). The applied bias was V_{ds} = 100 V with a quiescent current of only 5 mA/mm. All power sweeps were terminated at a transducer gain (G_T) compression of 3 dB. The maximum P_{out} with only fundamental tuning applied is 15.5 W/mm. When additionally terminating the second harmonic at input and output for optimal efficiency, the maximum PAE is 84.7 % at a P_{out} of 6.1 W/mm. Even at a considerably higher P_{out} of 11 W/mm, still 80 % of PAE are obtained. Terminating the second harmonic impedances results in almost 15 percentage points of improvement in PAE, of which 10 percentage points can be attributed to the second harmonic at the output, while the input second harmonic termination adds 5 percentage points.

At 7.2 GHz, a frequency band used for the Deep-Space Antennas, operated by the *European Space Agency (ESA)*, a 6x150 µm device was measured with fundamental tuning only up to 3 dB of G_T compression, using the same pulse conditions as for the 2.0 GHz measurement. The device delivers a maximum P_{out} of 13.8 W/mm and a PAE of 57.2 %.

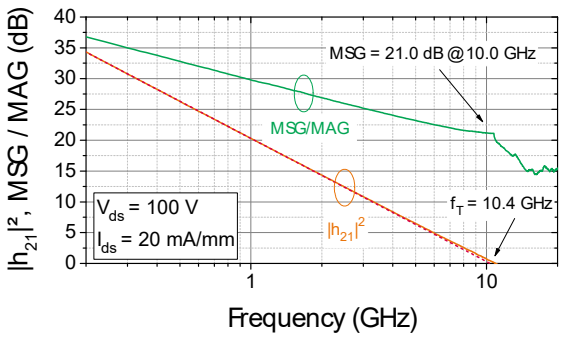


Fig. 6. MSG/MAG and $|h_{21}|^2$ of a 6x150 µm device, measured at V_{ds} = 100 V, I_{ds} = 20 mA/mm. The extraction of f_T has been done by fitting a -20 dB/dec slope to $|h_{21}|^2$ at 1.0 GHz.

When picking a trade-off load that combines good P_{out} with high PAE and additionally terminating the second harmonic at the output for maximum efficiency, a PAE of 66.0 % at a P_{out} of 10 W/mm is obtained. The power gain (G_P) is 18.5 dB, demonstrating the technology's superior performance at upper C-band frequencies. To the authors' best knowledge, the efficiency values, both at 2.0 GHz and 7.2 GHz, set a new record for GaN HEMTs operated at a V_{ds} of 100 V.

S-parameter measurements of the same 6x150 µm device performed at V_{ds} = 100 V and I_{ds} = 20 mA/mm, given in Fig. 6., yield a transition frequency (f_T) of around 10 GHz, when fitting a function with a -20 dB slope to the measured $|h_{21}|^2$ at 1.0 GHz. Despite the moderate f_T value, the device shows a maximum stable gain (MSG) of more than 21 dB at 10 GHz and a k-point, the intercept point of maximum stable gain and maximum available gain (MAG), of 10.5 GHz. The high supply voltage generates a large amount of voltage gain, making up for the limited current gain that is resulting from the thick barrier and long gate length. The demonstrated gain values are comparable with those, achieved by state-of-the-art 28-V 0.15-µm GaN technologies, proving the capability to operate the devices through X-band [6].

Conclusions

We demonstrate improvements in device efficiency of our 100-V GaN technology, which were achieved by careful tuning of the epitaxial structure as well as changes in the intrinsic device layout. Excellent electrostatic behavior is obtained, effectively suppressing short-channel effects. Revising the intrinsic device features leads to a 40 % reduction of output capacitance compared to the previous technology version. Combining that with the high gain of the devices, allows extending the applicable frequency range through X-band.

Furthermore, excellent large-signal results are demonstrated, reaching PAE values of 84.7 % at 2.0 GHz and 66.0 % at a frequency of 7.2 GHz. To the best of the authors' knowledge, both values set records for GaN HEMTs operated at 100 V.

Acknowledgements

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Acronyms

CPC: Copper, Copper-Molybdenum, Copper
CW: Continuous Wave
DC: Direct Current
DE: Drain Efficiency
DIBL: Drain-Induced Barrier Lowering
ESA: European Space Agency
HEMT: High-Electron-Mobility Transistor
MOCVD: Metal-Organic Chemical Vapor Deposition
MAG: Maximum Available Gain
MSG: Maximum Stable Gain
PAE: Power-Added Efficiency
STFP: Source-Terminated Field Plate
STS: Subthreshold Slope
TGW: Total Gate Width