# Electrical characteristics of Wavice GaN HEMT on 4” SiC with 0.2 µm gate process for X- and Ku- band applications

Junhyeok Lee, Min Han, Kyeongjae Lee, Byoungchul Jun, Seokgyu Choi, Jihun Kwon, Hankyul Ji, Chulsoon Choi, Hogeun Lee, and Sangmin Lee*

Wavice Inc., Hwasung-si, Republic of Korea
Email: jhlee@wavice.com, phone: 82-10-4754-5220
*Corresponding author

**Keywords: GaN, HEMT, Foundry, X-band power amplifier.**

**Abstract**

**The electrical characteristics of AlGaN/AlN/GaN High Electron Mobility Transistor (HEMT) on 4-inch high purity semi-insulating (HPSI) SiC substrates fabricated with a manufacturable 0.2 µm gate process of Wavice Inc. by using i-line stepper have been reported. The process of Wavice Inc. comprises $Al_xGa_{1-x}N$/AlN/UID-GaN/HR-GaN epi structure with x = 22 %, Si+ ion-implanted, and recess etched ohmic, void free source connected field plate (SCFP), 5 µm thick electro plated interconnect metal, 85 µm SiC substrate thickness after grinding, through SiC via directly to the source ohmic metal with sloped side wall, 7 µm thick electro plated back side metal. The fabricated devices exhibit power density of 5.48 W/mm with power added efficiency (PAE) of 55 % at $V_{ds}$ = 28 V. The $f_T$ and $f_{MAX}$ were measured as 32 and 75 GHz, respectively.**

## Introduction

There is an increasing demand for a high frequency solid-state power amplifier with high-power handling capability and smaller chip size in wireless communication and military applications. GaN-based HEMT on SiC, which is suitable for these applications due to superior material properties such as high current density, high thermal conductivity, and high breakdown field, have been widely used recently and have been rapidly replacing its counterparts such as LDMOS, magnetrons, and GaAs-based FET [1-4].

Wavice previously reported high performance and excellent reliability of 0.4/0.3 µm gate GaN HEMT on 4” SiC [1-2]. In this report, we present 0.2 µm GaN HEMT on 4” SiC for X- and Ku-band applications. 0.2 µm gate foot was realized by using i-line stepper, which is suitable for mass production. The fabricated devices exhibit high performances and excellent uniformity.

## Fabrication Process

Figure 1 shows (a) the picture of Wavice 0.2 µm GaN HEMT on 4” GaN-on-SiC wafer, and (b) the optical microscope image of a fabricated PCM device.

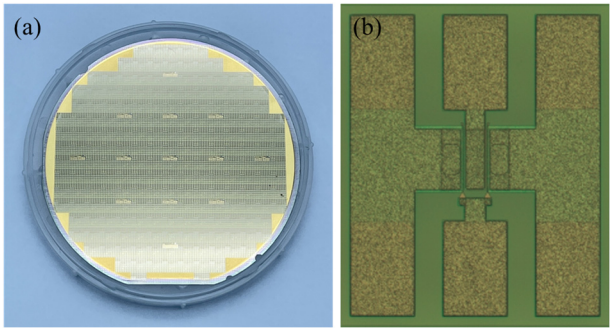


Fig. 1 Optical microscope images of (1) a GaN HEMT on a 4” SiC wafer and (b) a PCM device with the Wavice’s 0.2 µm GaN HEMT process.

$Al_{0.22}Ga_{0.78}N$/AlN/GaN (24 nm /1 nm/ 2 µm) epi structure was grown on HPSI 4” SiC substates by Wolfspeed, Inc. The sheet resistance of the epi structure was investigated by using Lehighton Electronics inc. LEI-1510EB. The epi structure exhibited $R_{sheet}$ of 340 Ω/sq. For device fabrication, Si-implanted and recess etched ohmic process was used. The 0.2 µm gate dimension was defined by i-line stepper photo lithography and inductively coupled plasma (ICP) etching through the $SiN_x$ passivation layer. Ni based Schottky gate metal was deposited by using an electron-beam evaporator, subsequently. Figure 2 (a), and (b) show the gate length uniformity map and the distribution chart of gate length across the 4-inch GaN-on-SiC wafer, respectively. The mean and the standard deviation of the gate length were 204 nm and 4.19 nm, respectively, which means excellent uniformity across the wafer.

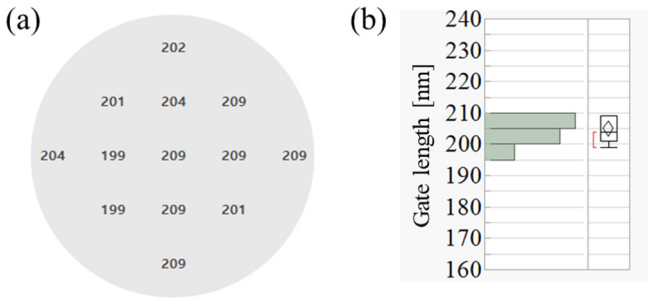


Fig. 2 (a) the gate length uniformity map, and (b) the distribution chart of the gate length across 4-inch wafer.

After depositing the second $SiN_x$ passivation layer, SCFP was formed with Au electro-plating. 5 µm thick Au interconnect metal was electro-plated as a final metal. The final $SiN_x$ passivation layer was deposited, and the pad region was defined by using ICP. When the front side process was completed, the backside of the wafer was thinned down to 85 µm by using mechanical polishing, and the through SiC via was formed directly to the source ohmic electrode. Finally, the backside metal was electro-plated with 7 µm thick Au. The cross-sectional SEM image of the fabricated device showing 0.2 µm gate electrode of Wavice GaN HEMT in this work is illustrated in Fig.3.

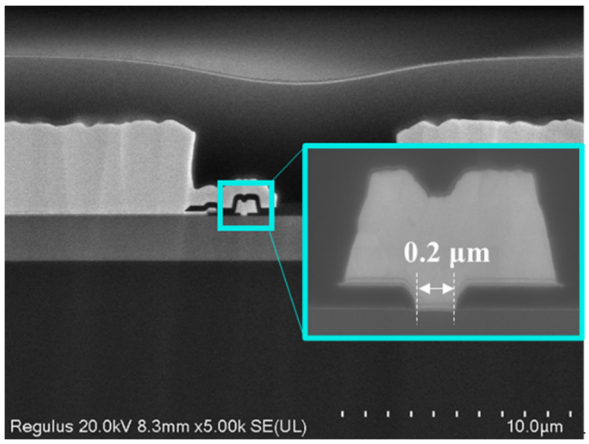


Fig. 3 The cross-sectional SEM image of 0.2 µm gate metal of the fabricated device with the electro-pated SCFP.

## Results And Discussions

The transmission line method (TLM) measurement is done on 13 process control monitor (PCM) devices with a HP4142B modular DC parameter analyzer. Figure 4 shows the TLM measurement results of the Si-implanted and recess etched ohmic contact. The average specific contact resistivity (SCR) of 2.2 × $10^{-6}$ Ω·$cm^2$, and the average sheet resistance of 458 Ω/sq are obtained as shown in Fig. 4 (a) and (b), respectively.

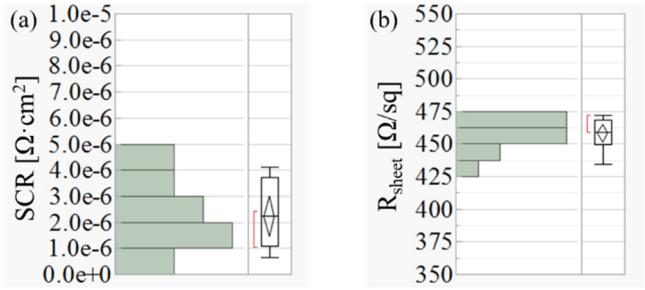


Fig. 4 (a) the specific contact resistivity (SCR), and (b) the sheet resistance of Si-implanted and recess etched ohmic contact, which is extracted from the TLM measurement on 13 PCM devices.

Transfer characteristics of the fabricated PCM devices are shown in figure 5. The drain-source distance of the devices is 4 µm, and the total gate width is 200 µm (2×100 µm). The devices exhibit the maximum drain current density ($I_{D,max}$) of 1.06 A/mm, and the maximum transconductance ($G_{m,max}$) of 355 mS/mm at $V_{GS}$ = −1.9 V and $V_{DS}$ = 10 V. The excellent device uniformity is observed with the standard deviation of 0.006 A/mm in $I_{D,max}$, and of 5 mS/mm in $G_{m,max}$ across the wafer. The average threshold voltage ($V_{th}$) is – 2.96 V, which is defined as the gate voltage when the drain current density reaches 1 mA/mm. The standard deviation of $V_{th}$ across the wafer is attained as 0.03 V. The distribution charts of $I_{D,max}$, $G_{m,max}$, and $V_{th}$ are shown in figure 6.

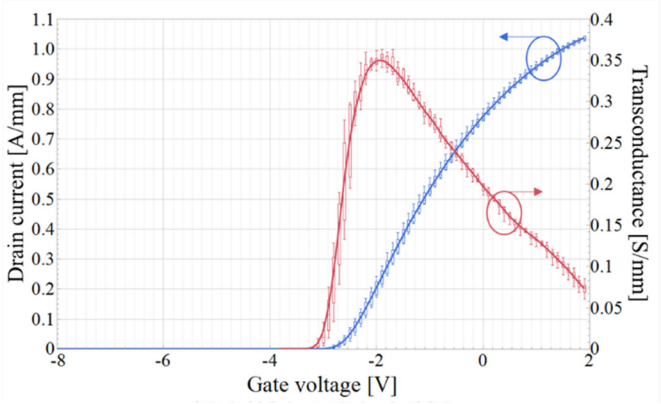


Fig. 5 Transfer characteristics of Wavice 0.2 µm GaN HEMT on 4" SiC at $V_{DS}$ = 10 V from GaN HEMT devices on 13 PCM sites. The line is the mean value and the bars the range of the data.

The off-state drain and gate leakage characteristics at $V_{GS}$ = −8 V are illustrated in figure 7. The average values of drain and gate leakage current at $V_{DS}$ = 10 V are 4.7 µA/mm and –2.2 µA/mm in average, respectively. The devices also exhibit excellent leakage characteristics at $V_{DS}$ = 100 V such as the mean values of 69 uA/mm on the drain −28 uA/mm on the gate at −8V of gate voltage.

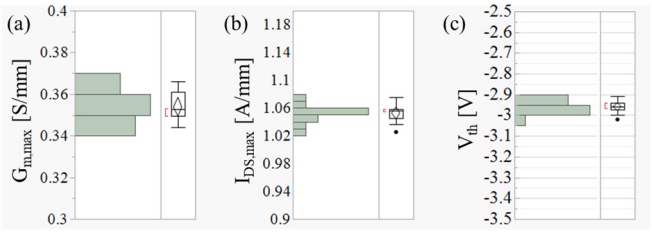


Fig. 6 The distribution charts of (a) maximum trans-conductance ($G_{m,max}$), (b) maximum drain current ($I_{DS,max}$), and (c) threshold voltage ($V_{th}$).

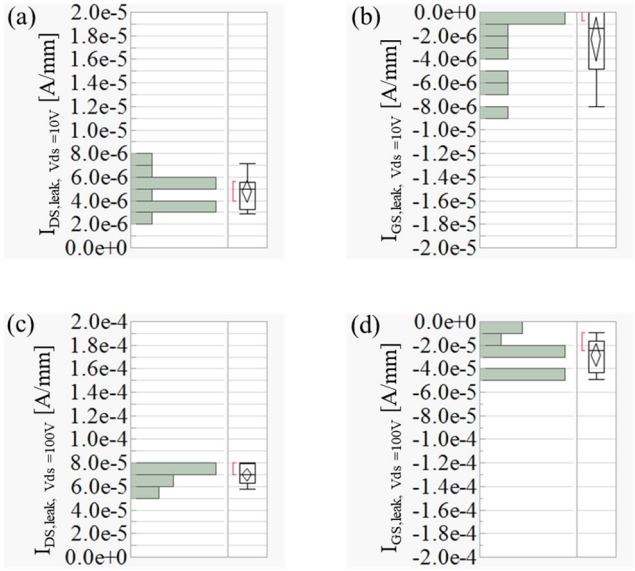


Fig. 7 The distribution charts of leakage current measured at $V_{GS}$ = − 8 V. (a) drain and (b) gate leakage current with $V_{DS}$ = 10 V, (c) drain and (d) gate leakage current with $V_{DS}$ = 100 V from 13 GaN HEMT devices with 200 µm total gate periphery.

The small signal RF performance for PCM devices is measured with Keysight N5222B network analyzer and Keysight B1505A power device analyzer. The unity current gain frequency ($f_T$) of 32 GHz, and the maximum oscillation frequency ($f_{MAX}$) of 75 GHz are achieved for these devices at $V_{GS}$ = −1.9 V and $V_{DS}$ = 20 V as shown in figure 8.

Figure 9 represents the load-pull performance at 10 GHz frequency of a typical PCM device which is tested by using Maury MT1000 series mixed-signal active load-pull system. The maximum PAE of 55 % at the output power of 30.4 dBm (power density = 5.48 W/mm) was attained at $V_{DQ}$ = 28 V and $I_{DQ}$ = 1 mA/mm. Table 1 summarizes the key DC and RF parameters for Wavice 0.2 µm gate GaN HEMTs in this work.

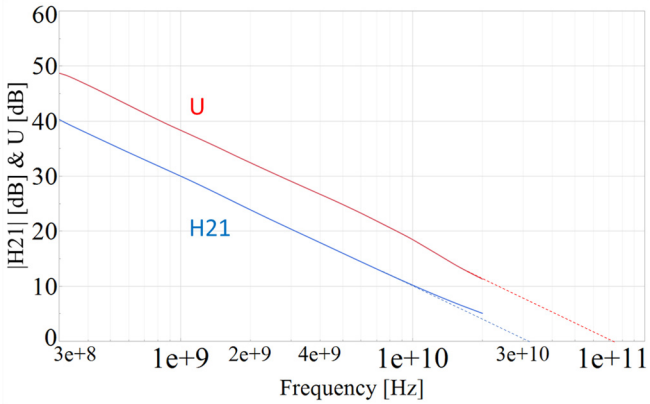


Fig. 8 |H21|, and Mason's unilateral gain against frequency for Wavice 0.2 µm gate GaN HEMT at $V_{GS}$ = − 1.9 V, and $V_{DS}$ = 20 V.

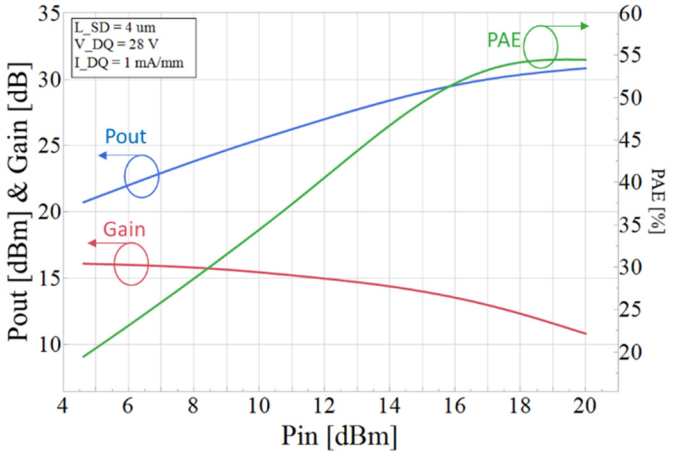


Fig. 9 10 GHz load-pull performance of Wavice 0.2 µm GaN HEMT on 4" SiC with $L_{SD}$ = 4 µm at $V_{DQ}$ = 28 V, and $I_{DQ}$ = 1 mA/mm.

TABLE 1 DC and RF performance from semiconductor parameter analyzer, small signal RF, and load-pull test on PCM devices.

| Test type | Characteristic | Condition | Unit | Typical |
|---|---|---|---|---|
| DC | $G_{m,max}$ | $V_{DS}$ 10 V, $V_{GS}$ – 1.9 V | mS/mm | 355 |
| | $I_{DS,max}$ | $V_{DS}$ 10 V, $V_{GS}$ 2 V | A/mm | 1.06 |
| | $I_{DS,leak,10}$ | $V_{DS}$ 10 V, $V_{GS}$ – 8 V | μA/mm | 4.7 |
| | $I_{GS,leak,10}$ | $V_{DS}$ 10 V, $V_{GS}$ – 8 V | μA/mm | – 2.2 |
| | $I_{DS,leak,100}$ | $V_{DS}$ 100 V, $V_{GS}$ – 8 V | μA/mm | 69 |
| | $I_{GS,leak,100}$ | $V_{DS}$ 100 V, $V_{GS}$ – 8 V | μA/mm | – 28 |
| | $V_{th}$ | $V_{DS}$ 10 V | V | – 2.96 |
| RF | $f_T$ | $V_{DS}$ 20 V | GHz | 32 |
| | $f_{MAX}$ | $V_{DS}$ 20 V | GHz | 75 |
| | $P_{sat}$ | $V_{DS}$ 28 V, Class B at 10 GHz | W/mm | 5.48 |
| | PAE | | % | 55 |

Based on these results, high power devices with wider gate periphery have been designed for large signal modeling and reliability test. Once the large signal model is made, the process design kit (PDK) with design manual, device model and passive components will be prepared for MMIC designers. The passive components such as metal insulator metal (MIM) capacitors, thin film resistors (TFR) and spiral inductors are described elsewhere. [5]

## CONCLUSIONS

In this work, excellent device uniformity and reasonably good electrical characteristics are observed from the fabricated devices on 4" GaN-on-SiC wafers with Wavice's 0.2 μm gate process by using i-line stepper photo lithography. These results demonstrate the feasibility of Wavice 0.2 μm technology for X- and Ku-band applications. Development of higher power devices and full qualification are in progress to provide foundry service.

## ACKNOWLEDGEMENTS

This work was supported by ICMTC (Institute of Civil-Military Technology Cooperation) of Korea under an ICMTC program (17-CM-MA-03)

## REFERENCES

[1] Sangmin Lee, et al., "*Qualification of Wavice Baseline GaN HEMT process with 0.4 μm gate on 4" SiC wafers"*, CS MANTECH 2020.

[2] Sangmin Lee, et al., "*Performance of 0.3 μm gate length GaN HEMT by using i-line stepper for high power C-band applications"*, CS MANTECH 2021.

[3] N. Miyazawa, M. Nishihara, K. Usami, M. Aojima, and T. Yamamoto, "*S-band 600 W and X-band 200 W high-power GaN HEMTs for radar transmitters*", SEI Tech. Rev., vol. 84, pp. 146–150, 2017

[4] M. Nishihara, M. Aojima, and N. Miyazawa, "*X-band 300 W High-Power GaN HEMT for Marine Radar Systems*", SEI Tech. Rev., vol. 91, pp. 29–32, 2020.

[5] Sangmin Lee, et al., "3.4 – 3.8 GHz 20W Compact 2-stage GaN HEMT Power Amplifier using IPDs on HPSI SiC substrates", to be published in CS MANTECH 2022.