Normally-off Millimeter-Wave InAlN/GaN HEMTs Fabricated by Atomic Layer Etching Gate Recess

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Abstract

In this article, we report on the high DC and RF performance of normally-off InAlN/GaN HEMT fabricated by atomic layer etching (ALE). An excellent gate-barrier layer interface is realized, including an off-state leakage of 2.7×10^{-2} mA/mm and smooth surface morphology has been achieved simultaneously. Atomic force microscopy (AFM) reveals a highly smooth interface morphology with an atomic layer etching root mean square (RMS) roughness of 0.62 nm. Compared with the traditional ICP etching, the atomic layer etching method improves the threshold voltage of the device without etching damage. Consequently, the enhanced device manufactured by the ALE process shows a high output current of >700 mA/mm and a threshold voltage of >0 V. In addition, the ALE-Normally-off InAlN/GaN HEMT with a gate length of 170 nm achieved f_T of 69 GHz and f_{max} of 100 GHz. These results show the great potential of the ALE process in promoting the development of radio frequency integrated circuits.

INTRODUCTION

With the development of high-voltage switches and high-speed RF circuits, enhanced GaN-based HEMTs have become a research hotspot in this field. The enhanced GaN-based HEMT only has an operating current when the positive gate voltage is added, which can greatly expand the application of the device in low-power digital circuits. [1] However, the research work of HEMT has also encountered many problems, one of which is that all HEMTs made by conventional processes are depleted. The depletion type HEMT is much more complicated than the enhanced HEMT circuit design, which increases the cost of the HEMT circuit. Enhanced HEMT is an important part of high-speed switching, high-temperature GaN integrated circuits, radio frequency integrated circuits (RFIC), and microwave monolithic integrated circuits (MMIC). From an application point of view, enhanced HEMT has an unparalleled advantage over depleted HEMT. In the field of microwave power amplifiers and low-noise power amplifiers, enhanced HEMT does not require negative electrode voltage, which reduces the complexity and cost of the circuit; in the field of high-speed RF switching, enhanced HEMT can improve the safety of the circuit; In digital fast circuit applications, nitride semiconductors cannot form complementary logic with low power consumption due to the lack of p-channel devices. Enhanced HEMT can alleviate the problem of lack of p-channels and achieve a simplified circuit structure.

The current methods for making enhanced devices include recessed gate structure making, thin barrier materials, p-GaN cap layer, F implantation, and so on. [2-5] These methods have their advantages and disadvantages, but for enhanced radio frequency devices, the advantages of recessed gates and strong polarization thin barriers are favored by major manufacturers and scientific research institutions due to their simple process and high reliability. [6] However, the recessed gate technology has very high requirements for the etching technology, which also leads to problems with the reliability and uniformity of the device. Especially for thin barrier materials with strong polarization, conventional etching techniques have large damage and the depth is not easy to accurately control. [7] These two problems need to be solved.

In this work, we fabricated a normally-off InAlN/GaN HEMT using atomic layer etching technology to test the DC and RF characteristics of the device and provided a control group of depletion devices. The analysis results show that ALE can effectively control the etching depth and reduce the etching damage, which provides a better processing method for the preparation of recessed gate enhanced devices.

DEVICE FABRICATION

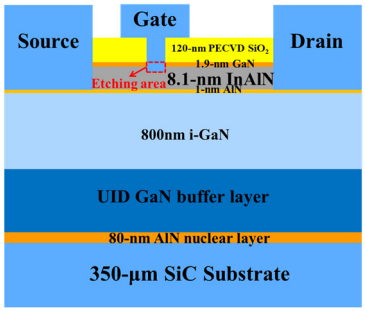

Fig. 1. Schematic cross-section of a recessed-gate InAlN/GaN HEMT.

InAlN/GaN epitaxial layers used in this work were grown on 3-in SiC substrates by molecular beam epitaxy, consisting

of an 80-nm-thick AlN nucleation layer, 2-μm-thick GaN unintentionally doped (UID) buffer layer, 800-nm-thick i-GaN buffer layer, 1-nm-thick AlN interlayer, and 1.9-nm-thick GaN cap layer on an 8.1-nm-thick $In_{0.17}Al_{0.83}N$ barrier layer. The Hall measurement at room temperature shows a sheet carrier density of 2.39 × 10^{13} cm^{-2}, mobility of 2008 $cm^2/V·s$, and sheet resistance of 131 Ω/sq. The source and drain ohmic contacts were fabricated with e-beam evaporation of Ti/Al/Ni/Au, lift-off process, and rapid thermal annealing at 820 ℃ in N_2 for 50 s twice. An ohmic contact resistance of approximately 0.43 Ω·mm was derived using the transmission line passivation with plasma-enhanced chemical vapor deposition (PECVD). The gate foot area was defined by removing the SiN layer with ICP etching in CF_4 plasma. CF_4/O_2 mixed plasma was used for depletion devices to etch SiN at a power of 80/10 W until SiN was completely removed. The ALE process was performed for recessed-gate devices: the interface was oxidized by O_2 plasma at 50/15W power for 10 s, N_2 was used to purge for 1 min, and then the oxide layer was removed by BCl_3 plasma at 50/15W power for 75 s， loop 10 times. Finally, 445-nm Ni/Au metal was evaporated to serve as a T-gate. The cross-section of a scaled recess-gate InAlN/GaN HEMT is shown in Fig. 1.

PROCESS ANALYSIS

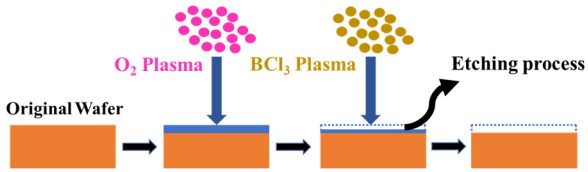

Fig. 2. Principles and steps of atomic layer etching

Q. Hu previously reported previously reported the use of O_2 and BCl_3 gas to achieve atomic layer etching in AlGaN/GaN system. [8] We chose this etching method in the InAlN/GaN material system and realized the end-to-end etching characteristics according to the different etching selection ratios of BCl_3 to oxide and nitride. The specific steps are shown in Figure 2: the original wafer was oxidized by O_2 plasma at 50/15W power for 60 s, N_2 was used to purge for 1 min, and then the Al_2O_3 and In_2O_3 mixed oxide layer was removed by BCl_3 plasma at 50/15W power for 75 s. Finally, N_2 was used to purge for 1 min to complete a single cycle. Atomic layer etching is composed of multiple cycles.

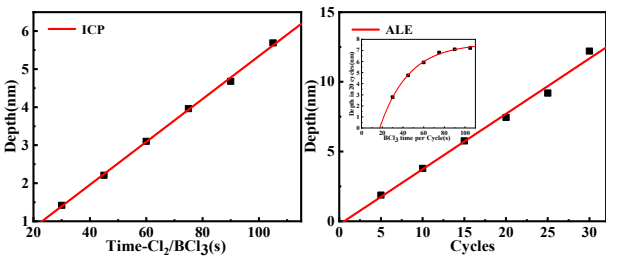

Fig. 3. Comparison of ICP etching rate and atomic layer etching rate

As shown in Figure 3, two different etching methods are used to compare the etching rate for the 5um line. The ICP etching depth changes linearly with the time of passing the Cl_2 and BCl_3 mixed plasma gas, and the slowest rate can reach 3 nm/min, but for thin barrier materials, the starting time will change slightly due to the unstable power matching time, thereby reducing the etching accuracy. For enhanced devices, the threshold voltage and saturation current need to be considered at the same time, and the critical point of the barrier layer thickness needs to be found. Therefore, ICP etching is not suitable for this more precise etching requirement. The ALE technology developed based on the InAlN/GaN material system ensures that the oxygen flow rate of each cycle is unchanged, and the time of BCl_3 is adjusted to ensure that the oxide layer can be carved out in each cycle. With the continuous increase of the time of passing BCl_3, the etching depth of 20 cycles gradually tends to be saturated, and it is measured that the final etching rate per cycle can reach 0.38 nm/Cycle. This technique is more suitable for thin barrier materials.

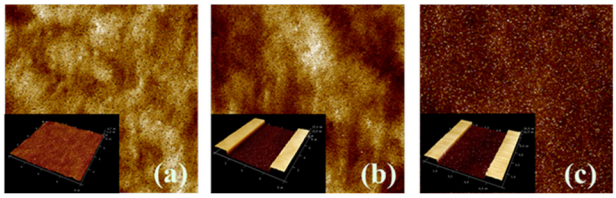

Fig. 4. AFM surface morphology (area: 8 × 8 μm2) of InAlN/GaN samples. (a) without etching (b) with ALE etching, (c) with ICP etching.

Fig. 4 shows the comparison of the AFM surface morphology of unetched, ALE, and ICP-etched samples. The root means square (RMS) indicates the roughness of the surface of the material. The larger the RMS, the more pronounced the undulation of the material surface and the higher the roughness. Large numbers of nanoparticles (black dots) are observed on the etched surface even after wet clean in organic solutions, resulting in an RMS roughness of 0.52 nm within the area of 8 × 8 $μm^2$. For the ALE-etched samples, an RMS of 0.62 nm was obtained. The ALE process can oxidize the surface of the material and etch the residue through low-power etching to ensure that the etched surface roughness is reduced and that the interface quality is improved. ICP etching treatment resulted in an RMS value of 1.39 nm. The impact of high-energy particles caused large fluctuations on the surface of the material, increased the interface damage, and affected the reliability of the device.

EXPERIMENTAL RESULTS

As shown in Figure 5, we performed DC tests on the D-MODE device and E-MODE device with a gate length of 170

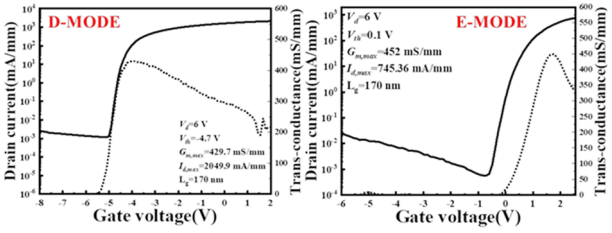

Fig. 5. Transfer curves of the depletion device and normally-off device by ALE etching

nm and a source-drain spacing of 3μm. For the D-MODE device, scan the drain current and transconductance curve of gate voltage from -8 V to 2 V under the bias voltage of V_d=6 V, the drain off-state leakage is 3.1E-3 mA/mm, and the drain saturation current It reaches 2049.9 mA/mm, the maximum transconductance is 429.7 mS/mm, and the threshold voltage obtained by linear extrapolation is -4.7 V. For enhanced devices, the off-state leakage is degraded: 2.7E-2 mA/mm, which is an order of magnitude higher than that of depleted devices. Linear extrapolation obtains a threshold voltage of 0.1 V, which is a positive drift of 4.8 V relative to the depletion-type device. The maximum transconductance is 452 mS/mm, and the drain saturation current is reduced to 745.36 mA/mm. As the thickness of the barrier layer under the gate decreases, the off-state leakage increases. The decrease in the drain saturation current is caused by the weakening of the polarization after the barrier layer is etched, leading to a positive drift in the threshold value and realizing enhanced devices' fabrication.

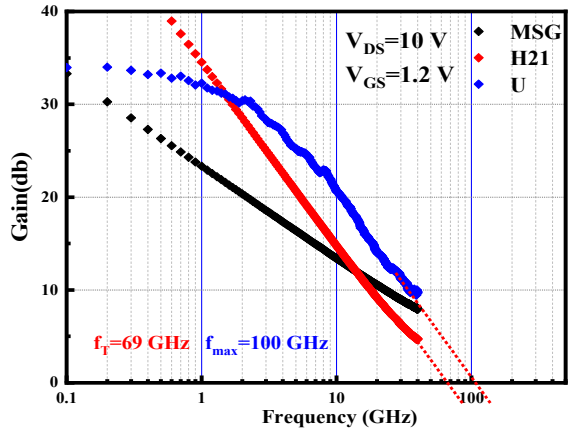

Fig. 6. Small signal characteristics of normally-off device.

As shown in Fig. 6, f_T/f_{max} of the normally-off device was 69/100 GHz, with the bias of V_{DS} = 10 V and V_{GS} = 1.2 V, respectively. It was demonstrated that the etching process didn't have an apparent influence on the small signal characteristic of the devices.

CONCLUSIONS

In conclusion, the ALE process is introduced in detail and enhancement-mode InAlN/GaN HEMTs are fabricated based on this method. The ALE-treated device has lower etching damage and better transport properties. For the ALE-treated device, this method can effectively reduce the damage of the etching interface, prevent the accumulation of impurity layers, effectively improve the performance of InAlN/GaN HEMTs, and provide an alternative for the development of high-frequency and high-power devices.

ACKNOWLEDGEMENTS

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ACRONYMS

ICP: Inductively Coupled Plasma
ALE: Atomic Layer Etching
AFM: Atomic Force Microscope
HEMT: High Electron Mobility Transistor