Leveraging microLED display technology to solve the chip-to-chip data communication bottleneck

Bardia Pezeshki

AvicenaTech Corp., 1130 Independence Ave, Mountain View, CA94043, www.avicena.tech

Keywords: MicroLED, multicore fiber, optical interconnects

Abstract

MicroLED displays fabricated on silicon ICs can form highly parallel datalinks in a spatially multiplexed format. Such a wide low-power data bus can address one of the biggest pain-points of the $400B IC industry. We demonstrate high speed microLEDs transferred onto silicon CMOS circuitry that includes integrated drivers for the LEDs, integrated Si detectors, and amplifiers. These chips are shown to operate at Gb/s speeds and can be interfaced with multicore fibers to make simple low-cost data-paths between standard silicon ASICs. We demonstrate these links using 130nm CMOS process, with <2pJ per bit and show their superior performance compared to FP lasers in terms of BER and mode partition noise.

INTRODUCTION

Almost all advanced ICs have wide internal busses that transfer data at modest rates within the chip. However, to connect to the outside world, these wide busses must be serialized into a few lanes to accommodate the limited number of signal pins available. The very high-speed SerDes (Serializers/De-serializers) to multiplex the data into these few lanes limit the reach of the signals across the circuit boards and cables, introduce distortions and errors that must be electronically compensated, consume a great deal of power, and add latency that limit compute architectures.

A technology that could connect the wide relatively slow internal busses of ICs (typically operating at a few Gb/s) with high I/O density would eliminate the need for the SerDes, dramatically reduce the power consumption of advanced ICs, enabling new architectures that require much higher levels of connectivity and low latency.

The display world has been developing GaN microLED technology where millions of LEDs are transferred onto silicon or glass backplanes. Aimed for mobile or headset applications, these displays outperform OLED or liquid crystal-based displays in terms of brightness, reliability, and energy efficiency. These same devices have also attracted attention for for LiFi and chip-to-chip data communication applications [1]. Devices optimized for speed can have electro-optical bandwidths of > 1GHz and can carry data at 10Gb/s per lane with simple equalization [2]. This is above the internal transfer rates of ASICs and well-matched for chip-to-chip application requirements.

APPROACH

Leveraging display industry advances, we proposed a new data communication architecture we call LightBundle™, where a large number of microLEDs transferred onto silicon ICs send optical data in a wide parallel format. The architecture, shown in Fig. 1, may use either a separate optical transceiver array chiplet or the optical transceiver array could be integrated directly onto the System-on-Chip (SoC). Each

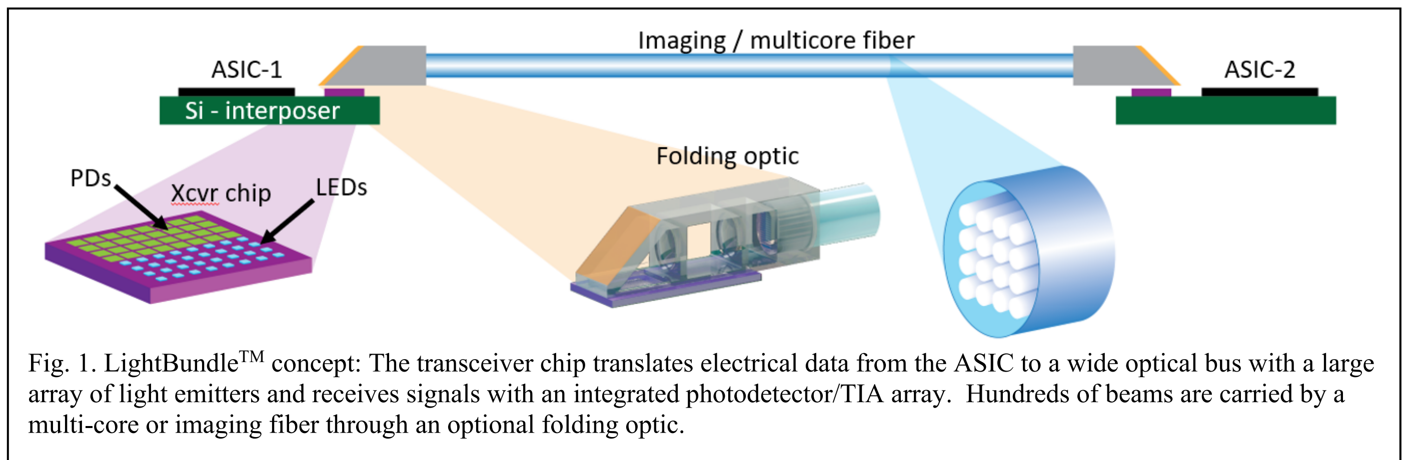

Fig. 1. LightBundle™ concept: The transceiver chip translates electrical data from the ASIC to a wide optical bus with a large array of light emitters and receives signals with an integrated photodetector/TIA array. Hundreds of beams are carried by a multi-core or imaging fiber through an optional folding optic.

optical transceiver array consists of hundreds of optical transmitters and receivers, where each optical transmitter includes drive circuitry and a microLED, and each receiver consists of a photodetector monolithically integrated with receiver circuitry onto a silicon IC.

The large number of lanes in a typical LightBundle interconnect can be carried using an imaging fiber [3] at very high density. Such a wide optical bus can connect to other ASICs or memory without the normal latency and power consumption associated with the current electrical links and release the current data bottleneck in advanced computing systems.

The LightBundle GaN microLEDs typically emit blue light in the 400 – 450 nm wavelength range. One advantage of this short wavelength light is the high performance that can be obtained with integrated photodetector/TIAs in silicon. The short absorption length of blue light in silicon enables photodetector (PD) structures that have very low capacitance per unit area [4]. The low capacitance allows high transimpedance gain in the TIAs which enables excellent sensitivity and very low power consumption, while the large area of the detectors eases alignment tolerances and thus reduces packaging cost.

In this work, we demonstrate LightBundle links at 2pJ/bit. In addition to very low power, we also show that these links do not suffer from the BER floors often observed in laser-based links. We also present a modest 32-element transmitter and receiver array on a custom silicon IC made with a 130nm process. The transmitter arrays are formed by transferring GaN microLEDs onto the IC. Under each LED is the drive circuitry, while the receive side of the chip contains 32 lateral p-i-n photodetectors with interdigitated electrodes integrated with TIAs and limiting amplifiers. We have previously shown the use of multi-core or imaging fibers that can carry hundreds of lanes simultaneously in a thin 0.5 - 1mm diameter imaging fiber. Both glass or plastic imaging fibers are suitable for this application and have similar performance in terms of loss (~0.2dB/m) and dispersion (~10m link for 4Gb/s per lane).

EXPERIMENTS

We demonstrated a low power microLED-based link operating at 2Gb/s with simple on-off modulation. The transmitter used a 15µm diameter microLED lifted-off and transferred to a silicon substrate that was modulated with a PRBS signal with about 0.7mA drive current. The receiver consisted of an integrated photodetector with TIA fabricated in a 130nm process by XFAB [5]. The PD was fabricated during the standard CMOS process using the source-drain implant/diffusions; thus, no additional process steps were needed. The n-well and p-well process steps were blocked, leaving behind the low doped bulk silicon substrate as the absorption layer. The diameter of the PD is 15 µm, and the spacing between the fingers of the interdigitated PD is 2.5µm. Photogenerated carriers in the intrinsic region move laterally towards the p and n fingers generating photocurrent. A TIA and limiting amplifier stage increase the received signal to CMOS logic levels. One advantage of these lateral detector structures is the very low capacitance per unit area. Both simulations and measurements indicated a total capacitance of less than 10fF for this device.

The transmitted light was passed through a variable attenuator and coupled to this integrated detector/TIA, generating about 1µA of photocurrent with no attenuation. The total power consumption of the light source at 2Gbps is about 1.5pJ/bit, while the entire receive chain consumed at 0.5pJ/bit (not including the 50Ω output driver). Thus, the total link power consumption was under 2pJ/bit. Fig. 2 shows the receiver output electrical eye. The right-hand side is the waterfall curve going down to 10^{-14} BER, and showing 10^{-12} BER at a sensitivity of < -21dBm.

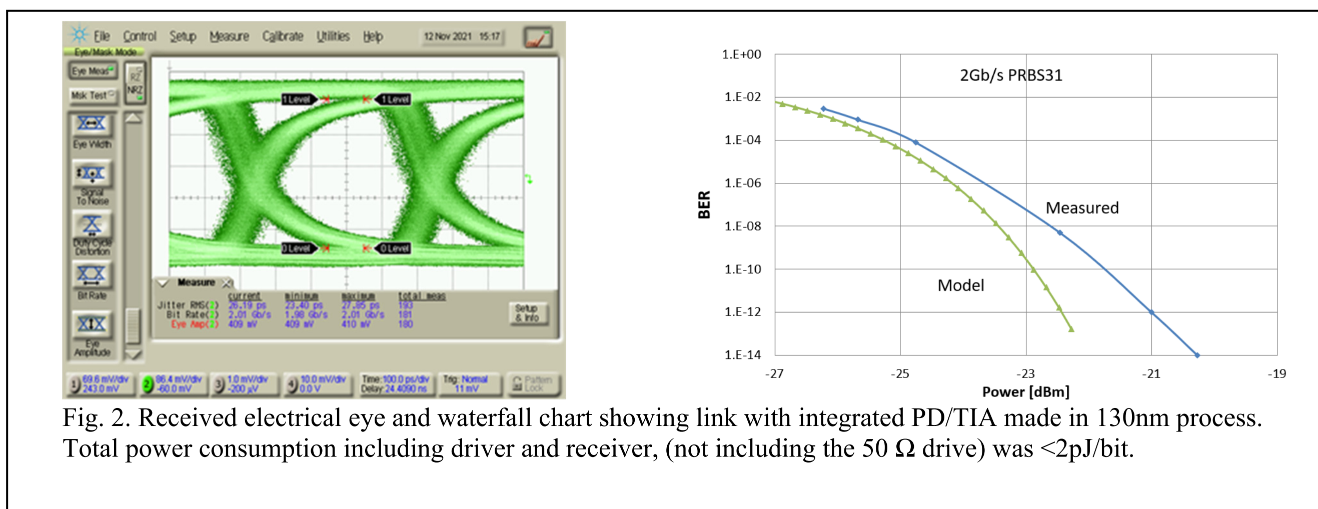

Fig. 2. Received electrical eye and waterfall chart showing link with integrated PD/TIA made in 130nm process. Total power consumption including driver and receiver, (not including the 50 Ω drive) was <2pJ/bit.

The error rate measured was limited by the power received on the photodetector. Driving the microLED at higher current levels and reducing the speed improved the BER, but of course the better BER consumed greater energy per bit. In general, we do not observe any BER floors, which is expected with LED-based links. By contrast, laser-based optical links tend to suffer optical coherence-based impairments such as modal noise, reflection, and frequency-to-amplitude noise conversion due to interferometric effects. The emission spectrum of our microLEDs is about 20nm centered at 430nm, and LED-based links do not require isolators, polarization control, or sophisticated modulation or error correction. The insensitivity of an incoherent source to feedback, stray reflections or other interferometric effects not only reduces the cost of the components and eases packaging, but makes them more insensitive to environmental effects.

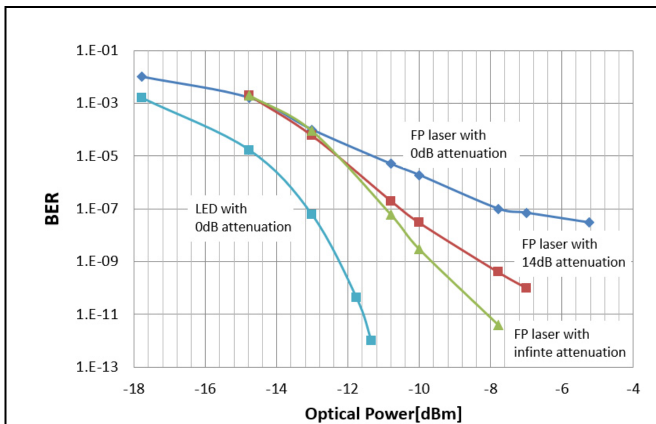

Fig. 3. BER of a microLED link versus F-P laser when there is interference, varying the attenuation in the interfering arm. MicroLED link shows superior BER even with no attenuation in the interfering signal, while the laser BER degrades rapidly.

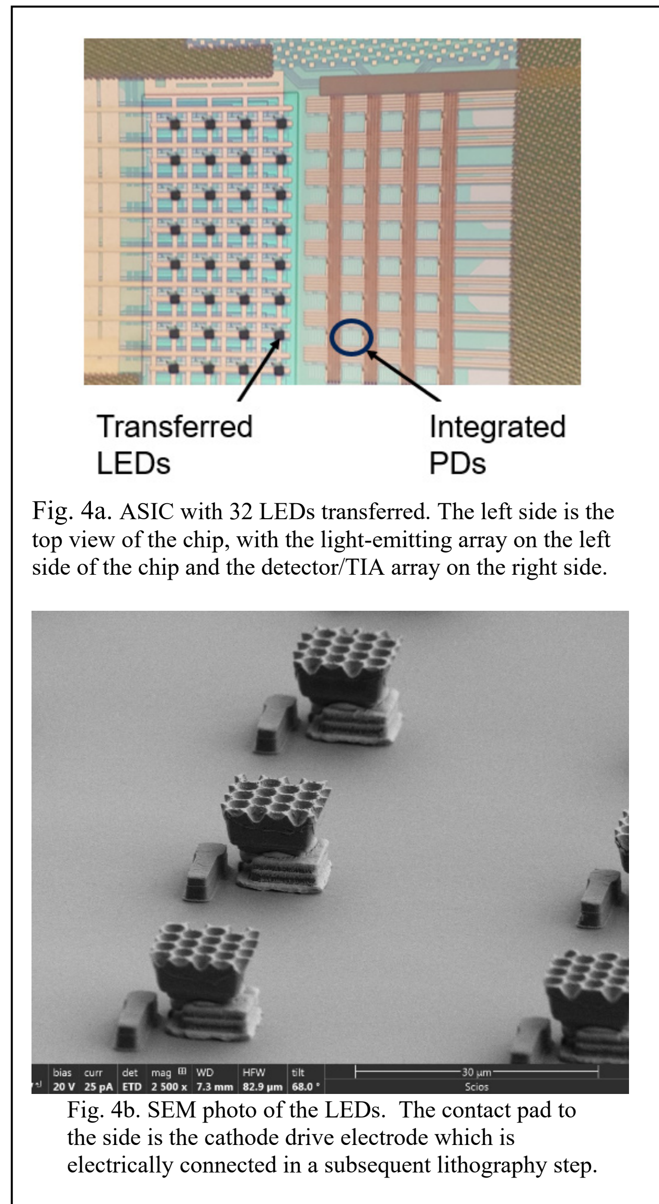

Fig. 4a. ASIC with 32 LEDs transferred. The left side is the top view of the chip, with the light-emitting array on the left side of the chip and the detector/TIA array on the right side.

Fig. 4b. SEM photo of the LEDs. The contact pad to the side is the cathode drive electrode which is electrically connected in a subsequent lithography step.

To demonstrate the robustness of LED-based links compared to laser-based, we set up a free-space Michelson interferometer and measured the BER as a function of the attenuation in one of the arms. We compared link performance for a microLED source to that for a blue Fabry-Perot edge-emitting source. In this case, a separate detector/TIA was used. Fig. 3 shows the BER as a function of received optical power as one of the interferometer arms is attenuated. The microLED-based link performance is insensitive to the interferometer configuration. By contrast, the BER of the FP laser-based link is dramatically worse when the power in the interferometer arms is roughly equal, showing the sensitivity of laser-based links to interference effects. Robust links that have fundamentally low BERs are critical in compute interconnects such as inter-processor or processor to memory links.

We previously demonstrated an eight-channel link in a fiber with ~50µm spaced channels that used separate driver ICs and TIAs [6]. This hybrid approach was limited by the number of channels and also in power consumption by the discrete 50Ω terminated discrete datacom ICs. To demonstrate a higher level of parallelism, we also fabricated a 130nm driver array and detector array in the previously mentioned XFAB's 130nm SOI process with 32 channels. Fig. 4a shows the image of an almost completed chip with the array of high speed GaN microLEDs. The GaN devices were grown on a sapphire substrate and processed into mesa structures with top p and bottom n contacts. The microLEDs array chip was then diebonded upside down onto the silicon ASIC using AuSn solder. Finally, the sapphire substrate was removed with a laser lift-off (LLO) process using a short

wavelength excimer pulse. This diebonding/LLO process is used by a number of GaN microLED displays companies and such processes can transfer millions of LEDs simultaneously. Subsequently, our demonstration chip underwent another lithography stage where the top n-contact was electrically connected to a second pad on the ASIC for the cathode that has the high-speed drive.

Fig. 4b is an SEM micrograph of the LED on the ASIC, once again just prior to the last lithography stage. The tops of the transferred LEDs have the checkered patterning of the patterned sapphire substrate (PSS).

The robustness and fundamentally low power consumption of microLED based links are very attractive for short-distance (< 10 meter) chip-to-chip interconnect applications. By comparison, other optical transceiver-based links are generally >10pJ/bit, while even the most advanced silicon photonics links aim for ~5pJ/bit [7]. Though the reach of single-mode fiber-based links far exceeds what can be achieved with microLEDs, they may be overkill for short distance applications. In this demonstration, the optical loss was higher than optimal, and thus the LED was driven quite hard. By improving the optical coupling and the LED structure (including an optimized back-reflector and light extraction), optical efficiency can be improved > 10dB. On the receive side, an optimized process on a more advanced node would further reduce the receive power consumption. By properly optimizing the microLEDs and the receivers in an advanced node, microLED-based links can achieve total power consumption in the ~0.1pJ/bit range, with costs an order of magnitude lower than other optical or electrical approaches, making them very attractive for shorter distance data interconnects.

Conclusions

We show GaN microLED based links are capable of very low power consumption and low BER. The short wavelength is ideal for integrated silicon detectors with TIAs. Such an approach can provide high density, low power consumption, and low latency for advanced computing applications.

References

[1] S. Rajbhandari et al., "A review of gallium nitride LEDs for multi-gigabit-per-second visible light data communications," Semicond. Sci. Technol. 32 023001 (2017).

[2] B. Pezeshki et al., "Wide and parallel LED-based optical links using multi-core fiber for chip-to-chip communications," Optical Fiber Conference (OFC 2021)

[3] H. Kosaka et al., "A two-dimensional optical parallel transmission using a vertical-cavity surface-emitting laser array module and an image fiber," IEEE Photon. Technol. Lett., 9, 253-255 (1997).

[4] A. Bhatnager et al., "Pump-probe measurements of CMOS detector rise ime in the blue," J. Lightwave Technol. Vol 22 (9) p. 2213-2217 (2004)

[5] F.Khoeini et al., unpublished.

[6] B. Pezeshki et al. "8x2Gb/s LED-based optical link at 420nm for chip-to-chip applications," 2021 European Conference on Optical Communications (ECOC21)

[7] M. Wade et al., "An error-free 1Tbps WDM optical I/O chiplet and multi-wavelength multi-port laser," Optical Fiber Conference (OFC 2021).