Impact of Strain-Induced Wafer-Bow on the Manufacture of VCSELs Grown on 150mm GaAs and Ge substrates

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Abstract – Strain-induced wafer bow of VCSEL epistructures on 150 mm GaAs and Ge substrates is measured and the effect on fabrication uniformity and yield is discussed. The spatial variation in oxidation length due to wafer bow is assessed and compared to that driven by compositional and thickness non-uniformity in the buried high-Al content layer.

INTRODUCTION

Due to the expanding VCSEL market, in recent years wafer manufacturers have scaled-up production using larger diameter substrates. Most often, VCSEL epi-structures for high-volume manufacture are grown on 150 mm GaAs substrates. However, at this diameter, the effects of strain-induced wafer bow become apparent, and manufacturing processes need to be adjusted to compensate. Further, as suppliers look to move to 200 mm substrates to meet demand [1] there are significant potential advantages for growth on Ge substrates.

Here, the wafer-scale fabrication and device uniformity for nominally identical epi-structures grown on GaAs and Ge substrates is compared. The spatial variation in oxidation length is quantified due to strain-induced wafer bow/warp on GaAs substrates is also presented.

One of the key processes for the production of VCSELs is the definition of the oxide aperture. The process of wet thermal oxidation of thin layer AlGaAs is has an exponential dependence on temperature [2] and, as such, a small temperature variation can result in a significant difference in oxidation length across the wafer. Key operating characteristics of VCSELs are highly dependent on the lateral dimensions of the active volume, hence a deviation from the desired oxidation length results in a significant variation in final performance. For oxidation furnaces that rely on thermal contact with a heated chuck for temperature control, the bow/warp of a GaAs substrate wafer leads to a non-negligible difference in temperature between the centre

and edge of a 150 mm wafer, which impacts the oxidation rate and must be compensated for in the manufacturing process.

Due to its elemental nature, the strain in large diameter Ge substrates is negligible in comparison to GaAs, therefore, the resulting wafer bow/warp is much less prominent and, as a result, standard implementations of wet oxidation of VCSEL structures grown on Ge can be utilised.

Here, the wafer bow of AlGaAs-based VCSEL epi-structures grown on both GaAs and Ge substrates is also characterised and the impact on device fabrication and yield is assessed. Furthermore, there can be spatial variations in the composition and thickness of the high-Al content layer which are also important considerations for oxidation rate, hence, the impact of material variation, and the effect of these non-uniformities on final device apertures, is also considered.

WAFER PROCESSING

Fabrication is performed at the Institute for Compound Semiconductors cleanroom in Cardiff University, with wafers up to 150 mm diameter patterned on a SÜSS MicroTec MA6 Mask Aligner by contact lithography or using a MicroWriter ML3 Pro direct write optical lithography tool. The same size capabilities are available for dry etch, thermal oxidation, and PVD tools. These tools have been acquired to match industry standards and, as such, the processing techniques used are similar to those employed in commercial settings. An Oxford Instruments PlasmaPro 100 Cobra Plasma Etch Tool is used for mesa isolation by ICP etching with a Cl-based gas chemistry. The sidewall profile of an etched VCSEL mesa can be seen in the SEM image of Fig. 1.

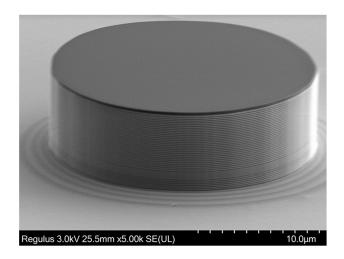


Fig. 1: SEM image of an ICP etched VCSEL mesa.

The ICP tool is equipped with in-situ monitoring by laser interferometry for control of etch depth into the VCSEL epistructure. Definition of the VCSEL aperture is achieved through thermal oxidation on an ALOXTEC Wet Oxidation Furnace. This furnace can process single wafers only with temperature control through contact with a heated chuck, but has the advantage of a vacuum atmosphere during ramp-up. The kit is equipped with real-time in-situ monitoring through an infrared camera, allowing measurements of oxidation length to be taken with an accuracy of \pm 0.5 μ m. Deposition of p- and n-type metal contacts is performed using a Kurt J Lesker PVD tool, equipped with both thermal and e-beam sources. Capability is being scaled up to process full 200 mm wafers, with state-of-the-art facilities to be housed in the Translational Research Hub, a development which forms part of a £300m Innovation Campus plan at Cardiff University.

MATERIALS AND METHODS

The epitaxial material in this study consisted of a MQW region situated in a λ -thick inner cavity sandwiched between an upper p-type AlGaAs DBR and a lower n-type DBR consisting of several pairs of AlGaAs layers with AlGaAs/AlAs pairs beneath for reduced thermal impedances. A buried Al $_{0.98}$ Ga $_{0.02}$ As layer was grown in the top DBR for definition of the oxide aperture. The epi-structures were designed for 940nm emission wavelength and were provided by IQE plc. Oxide confined VCSEL devices were produced using standard processing techniques.

The variation in oxidation length across an intact 150 mm GaAs substrate wafer is measured in-situ during the process. This is contrasted and compared with cleaved samples taken from the centre and edge of a wafer with a nominally identical epi-structure, also grown on a GaAs substrate. By

oxidising cleaved samples together in the centre of the furnace, the effects of wafer bow/warp are removed, thus isolating the effects of the epi-layer non-uniformity. The oxidation variation of a nominally equivalent VCSEL epi-structures grown on Ge is also measured. During processing, etch depth uniformity was measured by SEM imaging, and fabrication critical dimensions measured by optical microscopy. These quantities were compared for VCSELs grown on both GaAs and Ge substrate wafers.

RESULTS

For a full GaAs substrate wafer, the oxidation length is found to increase approximately radially and is longest at the edge – resulting in smaller oxide apertures away from the centre. A centre-to-edge variation in oxidation length of 3.1 μ m for a fully processed 150mm GaAs substrate, shown in Fig. 2.

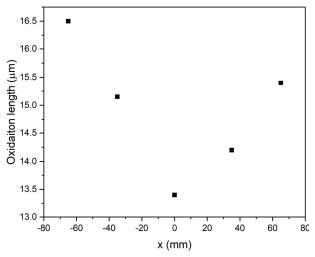


Fig. 2: Variation in oxidation length across a horizontal line profile of a 150 mm GaAs substrate wafer.

However, by measuring the oxidation length on cleaved material, the impact of the material variation is isolated. The resulting oxidation length as a function of the radial position from the centre is shown in Fig. 3. For the cleaved samples, there is a -2.2 μ m centre-to-edge variation in the oxidation length for 22.5 μ m mesas. When processed as a full wafer there is an increase in oxidation length towards the edge, however, this is a decrease in oxidation length when the impact of wafer bow/warp is removed. Therefore, the effect of the bow/warp is so significant that it dominates over the effect of the compositional and thickness variations of the buried high-Al composition oxidation layer.

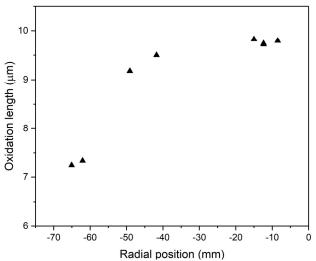


Fig. 3: Oxidation length variation for samples taken from the centre and edge of a 150 mm GaAs substrate wafer. Measurements were made on 22.5 μ m circular mesas.

The impact of this oxidation length non-uniformity on laser performance is shown in the wafer map of threshold current for 38 μ m mesas in Fig. 4. There is an approximately radial decrease in threshold current for VCSELs grown on GaAs, which matches the trend with oxidation length.

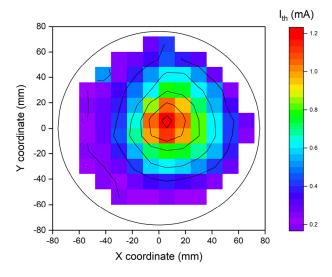


Fig. 4: Radial variation in threshold current of 38 μ m mesa VCSELs across a 150 mm GaAs substrate wafer.

Therefore, it is clear that the strain-induced wafer bow/warp for VCSEL structures grown on GaAs substrates leads to a spatial non-uniformity in device performance when processed as a full wafer. In Fig. 5, the measured bow/warp of nominally identical VCSEL epi-structures grown on both GaAs and Ge substrates are shown. This measurement was performed using the auto-focus function of the direct write

optical lithography tool and has an error of 1 μ m. The convex bow of the GaAs substrate can be clearly seen, with an effective height difference of the centre and edge at approximately 160 μ m. The Ge substrate, on the other hand, exhibits a slight saddle-shape, with virtually no height difference, in comparison. The observed undulations likely result from pre-growth polishing of the substrate.

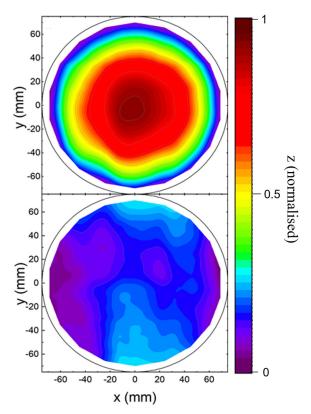


Fig. 5: Contour plots showing the relative wafer bow/warp of VCSEL structures on GaAs (top) and Ge (bottom) substrates

The superior uniformity of structures over a 150 mm wafer grown on a Ge substrate leads directly to improved fabrication uniformity and this translates into uniformity of final device performance. This advantage makes Ge the ideal substrate for high-volume manufacture of VCSELs and would provide a straightforward transition to 200 mm wafers, without the need for compensation in processing techniques.

CONCLUSION

The limitations of high-volume manufacture of VCSELs grown on GaAs substrates associated with strain-induced wafer bow/warp have been presented. This is compared with growth of VCSEL epi-structures on Ge substrates, where the greatly reduced wafer bow leads to advantages in fabrication

uniformity, and hence, will lead to greater uniformity in final device performance and higher manufacturing yield.

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ACRONYMS

VCSEL – Vertical cavity surface emitting laser

MQW – Multiple quantum well

DBR – Distributed Bragg reflector

PVD – Physical vapour deposition

SEM – Scanning electron microscope