SiC device manufacturing and road to volume production

Victor Veliadis
Executive Director and CTO, PowerAmerica, Raleigh, NC USA
Professor in Electrical and Computer Engineering, North Carolina State University

E-mail: jvveliad@ncsu.edu, +1-443-255-9899

Keywords: substrate, fabrication, heated implantation, Ohmic contact, silicide, SiC fab infrastructure

Abstract

Silicon (Si) power devices have dominated power electronics due to their low cost volume production, excellent starting material quality, ease of fabrication, and proven reliability. Although Si power devices continue to improve, they are approaching their operational limits primarily due to their relatively low bandgap, critical electric field, and thermal conductivity that result in high conduction and switching losses, and poor high temperature performance. Silicon Carbide's (SiC) compelling efficiency and system benefits have led to significant development efforts over the last two decades and today planar and trench MOSFETs, and JFETs are commercially available from several vendors as discrete components or in high power modules in the of 650 V to 1700 V voltage range. As SiC continues to grow, the industry is lifting the last barriers to mass commercialization that include higher than Si device cost, the presence of basal plane dislocations, reliability and ruggedness concerns, and the need for a workforce skilled in SiC power technology to keep up with the rising demand. In this paper, we will review key aspects of SiC technology and discuss overcoming barriers to mass commercialization.

SiC Wafers

Currently, the SiC wafer represents 55-70% of the overall SiC device cost [1], a consequence of its unique complex fabrication specifics. Conventional SiC substrates are primarily grown by the seeded sublimation technique at temperatures of ~2500 °C, which creates process control challenges. Crystal expansion is limited requiring the use of large high-material quality seeds, and the sublimation growth rates can be relatively low in the order of 0.5-2 mm/h. Dislocations propagate through the boule and are present in the device wafers. Furthermore, SiC material's hardness, which is comparable to that of diamond, makes sawing and polishing SiC substrates slow and costly relative to Si.

The epitaxial layers, where SiC devices are fabricated, are grown by chemical vapor deposition (CVD) in horizontal or planetary reactors at 1500-1650 °C. Pressure typically ranges from 30 to 90 Torr and growth rates can be as high as 46 mm/hr. Epitaxial growth is done on 4-degree off-cut substrates to maintain the polytype stability of the substrate. Epitaxy goals are to restrict "performance-degrading" defect propagation from the substrate into the epitaxy and ensure that any "performance-degrading" defects propagating from the substrate propagate as benign defects into the epitaxy. As defects in SiC wafers limit large-area device yields, and numerous devices are paralleled in modules to increase current output, tight epitaxial doping and thickness uniformities are highly desirable, particularly as wafer size increases. Overall, SiC wafer fabrication is more complex and slower than that of silicon. The result is more expensive wafers, and ultimately higher device costs. A key part of the vertical integration occurring in today's SiC industry is securing internal substrate and epitaxy wafer capabilities to eliminate purchasing profit margins. In addition, opportunities for disruptive SiC substrate formation, boule slicing, sawing/polishing, etc., have a high return and are being sought by several companies.

Presently, the majority of SiC device production is on 150 mm wafers. 200 mm SiC wafers were demonstrated in 2015, and a seven-year or so period historically passes before they become available as products. It is highly desirable that defect density and the cost of material per cm2 are the same or lower for 200 mm vs. 150 mm wafers. In addition, wafer planarity should not be worse in the 200 mm wafers. Due to the large fab/foundry overheads, and assuming 200 mm tools are in place, the cost of processing a wafer is to a first approximation unrelated to its size. So processing a 200mm wafer will produce about 1.8 times more devices than a 150 mm wafer at the same processing cost. Of course, a 200 mm wafer will be more expensive than a 150mm wafer, and that needs to be factored into the overall cost equation. Many silicon fabs/foundries are starting to process SiC wafers as well, and given the plethora of 200 mm Si fabs/foundries with fully depreciated tools, there are many large 200 mm Si companies waiting on the sidelines to enter SiC production when 200 mm wafers become commercially available. These are companies that have established 200 mm silicon wafer production and do not want to retool to fabricate at the 150 mm SiC wafer size that is currently commercially available. Therefore, when 200 mm wafers become available, many 200 mm fabs/foundries will start producing SiC devices. To illustrate the economic benefits of moving to larger wafer size, let us assume starting material cost parity per cm² between 150 mm and 200 mm

wafers. Further assuming a $1500 cost for a fully processed 150 mm SiC wafer, and 60% of that coming from the starting wafer material (40% fabrication cost), a back of the envelope calculation points to a 17% device cost reduction when switching to 200 mm. The same fabrication cost scenario, with now 50% of the overall cost representing the starting wafer material, allows for a 22% device cost reduction when switching to 200 mm wafers. These calculations do not include additional processing cost reductions that will come with streamlined mass production in large 200 mm volume fabs/foundries.

SiC Device Fabrication

For mass SiC commercialization, high yielding fabrication processes are required. Numerous well-established processes from silicon technology have been successfully transferred to SiC. However, SiC material properties necessitate optimization of specific processes including wafer thinning, etching, heated implantation and anneal, and low resistivity Ohmic contact formation [2]. SiC is inert against chemical solvents and only dry etching is practical. Furthermore, the hardness of SiC results in low photoresist selectivity and a "hard" mask, usually composed of metal or dielectrics, is required for SiC photolithographic patterning and etch.

0.7 µm deep SiC mesas, trenched using a "silicon" reactive-ion etch (RIE) tool and a Cr/Al mask, are shown in Fig. 1. Cr assists with adhesion of metal layers to the underlying SiC surface. The RIE was fluorine- based for higher mask/SiC selectivity. RIE settings were optimized to eliminate micro-masking and achieve vertical etched sidewall profile formation.

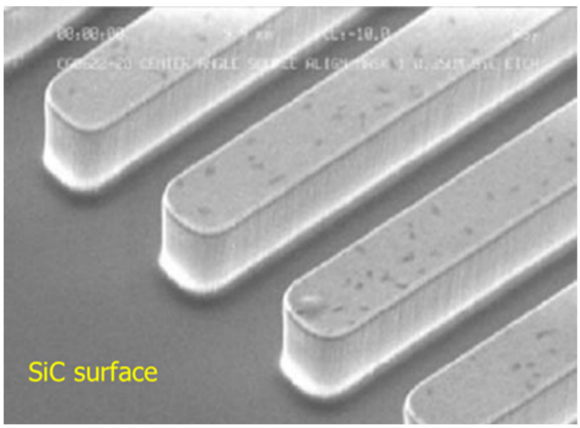

Fig. 1. Reactive-ion etched 0.7 µm deep vertical SiC mesas using a Cr/Al mask. Cr assists with adhesion of metal layers to the underlying SiC surface. The RIE was fluorine- based.

Conventional thermal diffusion is not realistic in doping SiC due to its high melting point and the low diffusion constant of dopants within SiC. Heated ion-implantation is typically performed for doping densities of 10^{16}-10^{20} cm^{-3} (the higher doping densities assisting with ohmic contact formation), and room temperature implantation can work well for low implant doses (~ 10^{15} cm^{-3}). Nitrogen/phosphorus and aluminum are the preferred impurities for n-type and p-type SiC doping, respectively. The as-implanted depth profiles are retained after the anneal for Al, P, and N as expected from their low diffusion constants. The lack of diffusion makes it easy to form shallow junctions and difficult to form deep ones. After ion implantation, a 1600-1800 °C anneal is performed for lattice damage recovery, and high dopant electrical activation. A protective cap layer covering the SiC wafer protects its surface from degradation due to Si desorption and migration of surface atoms, Fig. 2.

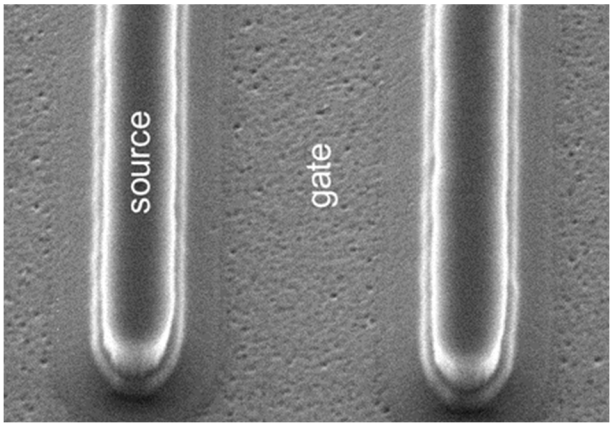

Fig. 2. Scanning electron microscopy image of a "post p+ ion-implantation" 1650 °C annealed SiC wafer in the presence of a carbon protective cap layer. Excellent surface morphology and high device yield are attained.

The high value of the SiC/metal barrier results in rectifying metal contacts and post metal deposition anneal is required for ohmic contact formation. Typically, a 50-100 nm Ni layer is blanket deposited and patterned on the wafer for the simultaneous ohmic contact formation on the n-type and p-type doped regions, Fig. 3. Depending on the specifics of the fabrication process, isolating the source from the gate areas with dielectrics can facilitate high yields in the subsequent high temperature processing.

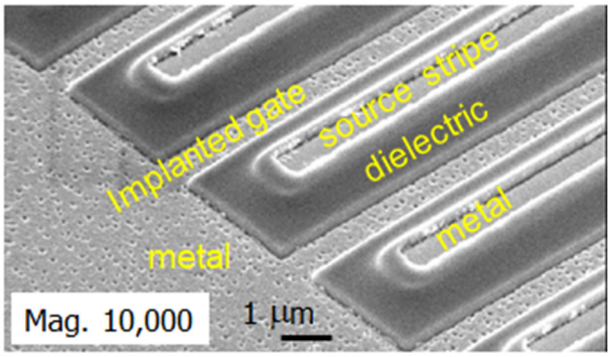

Fig. 3. Scanning electron microscopy image of a patterned Ni layer on a SiC wafer surface. Dielectric isolates the metalized p+ implanted gate areas (pitted surface) from the n-doped source stripes.

High temperature annealing of the Ni patterned wafer creates Ni-silicide for low resistivity ohmic contact formation. Rapid thermal annealing (RTA) at 950 °C, using standard silicon fabrication equipment, was used to create Ni-silicide with no metal strings, Fig. 4. The dielectric isolates the source from the gate areas eliminating shorting during the high temperature silicide process.

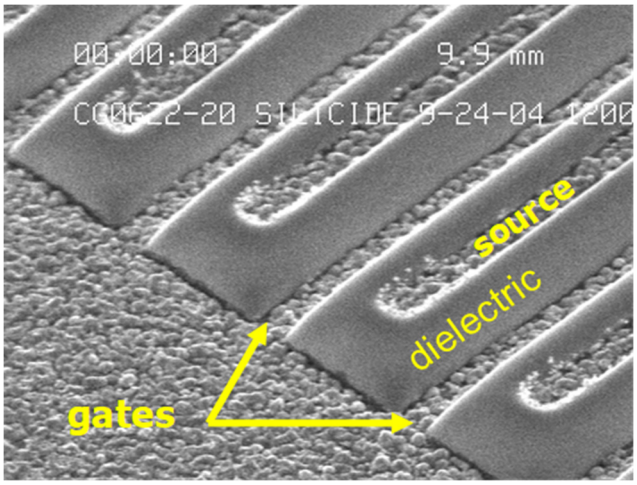

Fig. 4. Scanning electron microscopy image of the Ni patterned SiC wafer of Fig. 8, after a 950 °C rapid-thermal-annealing event. Ni silicide is formed with no shorting of the p-gate to the n-source regions.

Unlike Si wafers, SiC wafers are transparent. This complicates the use of "silicon" tools for CD-SEM and metrology measurements, as the focal plane is determined with the use of an optical microscope. SiC-specific wavelength metrology/inspection tools are now available from multiple vendors. Another issue is the relative lack of flatness of SiC wafers, compared to those of Si, which can complicate photolithography. In addition, the high-temperature SiC processing can further degrade wafer flatness, occasionally rendering wafers unusable. This is particularly problematic with the thick epitaxy wafers used in +3.3 kV device fabrication. Efforts are underway to produce flatter starting SiC wafers, and to minimize flatness degradation during fabrication. Lastly, the poor SiC/SiO2 interface quality reduces inversion layer mobility. Thus, passivation techniques including annealing in nitrides are utilized to improve the SiC/SiO2 interface quality similar to the case of silicon.

Device manufactures have developed IP for several SiC processing steps and compete on both design and processing. Although SiC is not fully CMOS-compatible, the SiC industry has leveraged Si technology processes and infrastructure by making the relatively small financial investments required to adapt existing fabs. Today, SiC manufacturing has matured and its fab infrastructure now mirrors that of Si. Integrated SiC device manufactures coexist with foundries and fabless companies, and design houses provide know-how and IP that can be leveraged to accelerate entry to market, Fig. 5.

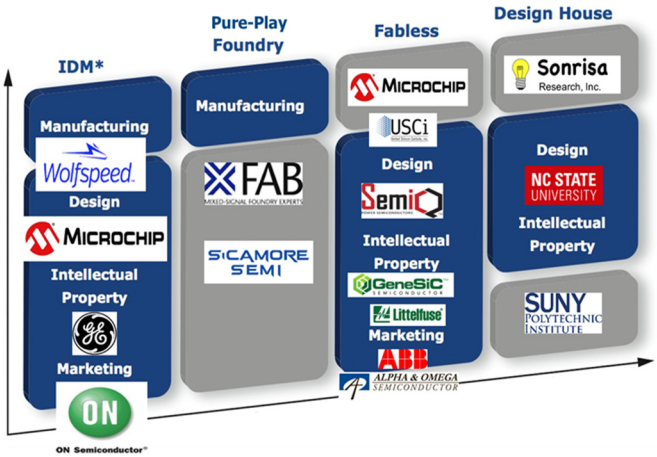

Fig. 5. The U.S. SiC fab infrastructure mirrors that of Si. It consists of Integrated Device Manufacturers, Foundries, Fabless companies, and Design houses.

SiC device fabrication in volume fabs alongside Si has emerged as a "cost reduction" model exploiting "silicon" manufacturing economies of scale. Through re-purposing older fully depreciated 150 mm (and 200 mm in the near future) Si foundries, SiC power devices can be manufactured with the relatively small investments necessary to support the unique SiC processing steps. Minimizing fabrication cost by exploiting the mature Si volume production assumes the fab is loaded close to capacity with standard Si and SiC processes running on the same lines. In addition, aggregating the demand for SiC substrates and epilayers in volume fabs contributes to lower material costs. Lower fabrication costs in a fully depreciated Si+SiC "capacity loaded" fab, coupled with decreased material costs can lead to significant price reductions for SiC devices. This approach offers a new opportunity for outdated Si foundries, which have not kept up with the channel length reductions of the last two decades, to continue manufacturing legacy Si parts while ramping up SiC fabrication that requires relatively modest ~0.3 micron design rules [3].

Defects, Reliability, and Ruggedness

The majority of "killer" defects have been virtually eliminated in modern SiC wafers. Basal-Plane-Dislocations (BPDs) are the major remaining defect degrading device performance [4]. BPDs can propagate from the wafer substrate through the thickness of the epitaxial layers where devices are fabricated. BPDs can also be generated during the high-temperature ion-implantation fabrication process. In commercial wafers, more than 95% of substrate BPDs propagate as relatively "benign" threading edge dislocations in epitaxial layers grown off axis by CVD [5].

When bipolar current flows through a SiC device, electron–hole pair recombination at BPDs in the drift layer provides the energy to activate dislocation glides that give rise to stacking faults and degradation. To investigate the impact

of BPDs on the electrical characteristics of ion-implanted SiC transistors 17 JFETs with 100-µm drift epilayers (10 kV rated) were stressed at a fixed gate-drain DC bipolar current density of 100 A/cm2 for 5 hours [6]. At 100 A/cm2, the gate–drain p-n junction is turned on, as evidenced by the emission of blue/violet electroluminescence at the edges of the JFET, and bipolar current flows. Of the 17 JFETs stressed, six exhibit no forward gate-drain voltage degradation. This confirms that with optimized process flows and implantation recipes, BPDs are not generated during fabrication.

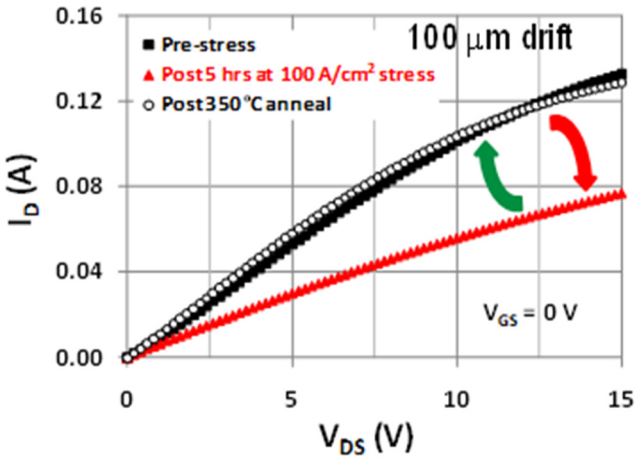

Fig. 6. BPD-related JFET ON-state conduction degradation and full recovery by annealing. The black squares, red triangles, and open circles represent the ON-state conduction characteristics prior to bipolar stress, after 5 hours of 100-A/cm^2 bipolar stress and after a 350 °C anneal, respectively.

Bipolar current in the presence of BPDs leads to forward gate–drain p-n junction and ON-state conduction degradations as shown in Fig. 6. Interestingly, transistor BPD-related electrical degradations can be fully reversed by annealing at 350 °C, while non-degraded characteristics remain unaffected by this annealing. Threshold voltage instability is the main remaining reliability concern in SiC MOSFETs, which are the dominant transistors in SiC-based power electronics applications. It is primarily due to oxide traps at the SiC/gate-oxide interface. A positive shift in the SiC transistor's threshold voltage has the deleterious effect of increasing conduction losses, while a negative shift is undesirable as it can spontaneously turn the device on. SiC devices can be made more rugged by leveraging design trade-offs. This, combined with intelligent gate drives, can provide adequate circuit protection [7-8]. Finally, a highly skilled workforce is key to creating increased device demand, which in turn, spurs SiC mass manufacturing and lowers overall costs. Entities like PowerAmerica carry out University/industry applied collaborative projects, offer industry-driven WBG short courses and tutorials at conferences, and match students with industrial internship opportunities [9]. These activities train the existing workforce and prepare the next generation of SiC technologists, facilitating accelerated deployment of SiC power electronics.

Conclusions

The compelling efficiency and system benefits of SiC are leading to wide adoption. Industry is removing the last barriers to mass SiC commercialization that include higher than Si device cost, the presence of basal plane dislocations, and reliability and ruggedness concerns. The wafer represents a disproportionately high percentage of the overall SiC device cost, compared to that of Si, and technological improvements and transition to volume 200 mm wafer production will help lower those costs. SiC manufacturing has matured, non-CMOS compatible processes are fully developed, and the SiC fab infrastructure mirrors that of Si. Basal plane dislocations are the major remaining yield lowering defect to overcome. Gate-oxide interface quality improvements will enhance performance and alleviate any lingering reliability concerns. A highly trained workforce that skillfully inserts SiC in systems is key to creating increased device demand, which in turn will spur SiC economies of scale.

References

[1] https://www.exa-watt.com/power-electronics

[2] V. Veliadis, Silicon Carbide Junction Field Effect Transistors (SiC JFETs), in: Wiley Encyclopedia of Electrical and Electronics Engineering, Online, 1 (2014).

[3] V. Veliadis, Compound Semiconductor Magazine 25, 36, (2019).

[4] E. Van Brunt, A. Burk, D. J. Lichtenwalner, R. Leonard, S. Sabri, D. A. Gajewski, A. Mackenzie, B. Hull, S. Allen, and J. W. Palmour, Mat. Sci. Forum 924, 137 (2018).

[5] T. Kimoto, Jpn. J. Appl. Phys. 54, 040103-1-27 (2015).

[6] V. Veliadis, H. Hearne, E. Stewart, M. Snook, W. Chang, J. Caldwell, H. Ha, N. El-Hinnawy, P. Borodulin, R. Howell, D. Urciuoli, and C. Scozzie, IEEE Elec. Dev. Lett. 33, 952 (2012).

[7] A. Kumar, S. Parashar, S. Sabri, E. Van Brunt, S. Bhattacharya, and V. Veliadis, IEEE 30th Inter. Sym. on Power Semiconductor Devices and ICs (ISPSD), 423 (2018).

[8] A. Kumar, A. Ravichandran, S. Singh, S. Shah and S. Bhattacharya, IEEE Energy Conversion Congress and Exposition (ECCE), 2560 (2017).

[9] V. Veliadis, IEEE Power Electronics Magazine, 62 (2019).