Device Figure of Merit Performance of Scaled Gamma-Gate β-Ga_2O_3 MOSFETs

Kyle J. Liddy[1*], Ahmad E. Islam[1], Jeremiah Williams[1], Dennis Walker[1], Neil A. Moser[1], Daniel M. Dryden[2], Nicholas Sepelak[2], Kelson D. Chabak[1], Andrew J. Green[1]

[*]E-Mail: kyle.liddy.1@us.af.mil

[1]Air Force Research Laboratory Sensors Directorate, WPAFB, OH, 45433

[2]KBR, Air Force Research Laboratory Sensors Directorate, WPAFB, OH, 45433

Keywords: β-Ga_2O_3, MOSFET, Figure of Merit, Scaled

Abstract

This work characterizes the Device Figure of Merit Performance of Scaled Gamma-Gate β-Ga_2O_3 MOSFETs. Reported is state of the art Baliga's Device Figure of Merit (BFOM) and record Dynamic switch Loss Figure of Merit for β-Ga_2O_3 devices, comparable to that of other state of the art compound semiconductor technologies. A minimum of 3 kV breakdown is achieved using both optical gates and gamma gates defined by EBL, reaching a voltage of operation not generally attainable through simple device topologies in other semiconductor technologies. This illustrates the potential for a β-Ga_2O_3 MOSFETs in switching applications.

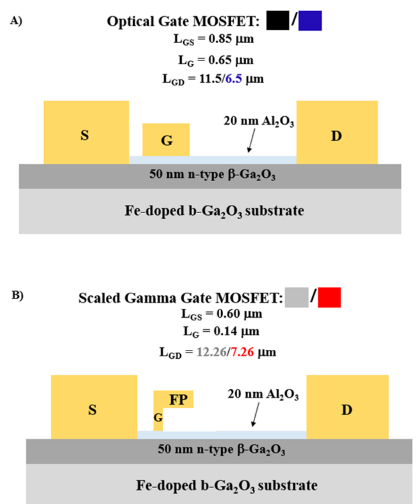

Figure 1 - Device cross section of optical gate (A) and Scaled Gamma Gate (B) MOSFETs with L_{GD} = 11.5 µm (black), 6.5 µm (blue), 12.26 µm (gray) and 7.26 µm (red)

INTRODUCTION

The dynamic switching loss figure of merit ($R_{ON}Q_G$ vs. V_{BK}) is a benchmark used to indicate a device's potential in power-switching applications. Similarly, the lateral Power Figure of Merit ($R_{ON,sp}$ vs. V_{BK}) indicates a devices conduction losses. To this point, many applications are dominated by Si CMOS, SiC and more recently GaN technologies. β-Ga_2O_3's unique properties, including a bandgap of 4.8 eV and an expected critical field strength of 8 MV/cm, make it an excellent candidate for next generation power-switching and high-voltage radio frequency (RF) applications. This work discusses the fabrication and FOM characterization of optical gate and EBL gate Ga_2O_3 MOSFETs and shows their potential for these application spaces that are currently dominated by other technologies. Until this point, dynamic switch loss analysis has only been reported in the literature by Chabak et. al. in 2018 [1]. Record Power Figure of Merit performance has been reported recently using a double heterojunction device design [2]. Multi-kV class MESFETs have also been reported in the literature achieving state of the art Power Figure of Merit performance [3]. Devices with 8 kV breakdown were recently reported [4], a record for Ga_2O_3 devices. The analysis performed within this paper resembles that performed by MIT in their

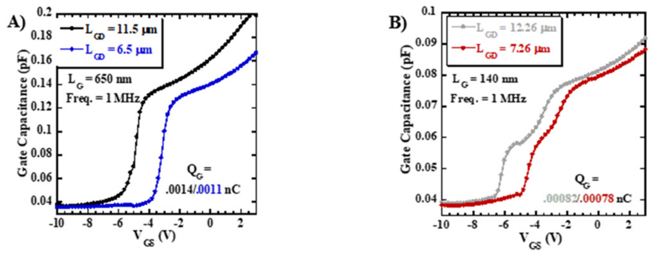

Figure 2 – Gate Capacitance (C_G) as a function of Gate-Source Voltage (V_{GS}) for optical gate (A) and Scaled Gamma Gate (B) MOSFETs with LGD = 11.5 µm (black), 6.5 µm (blue), 12.26 µm (gray) and 7.26 µm (red)

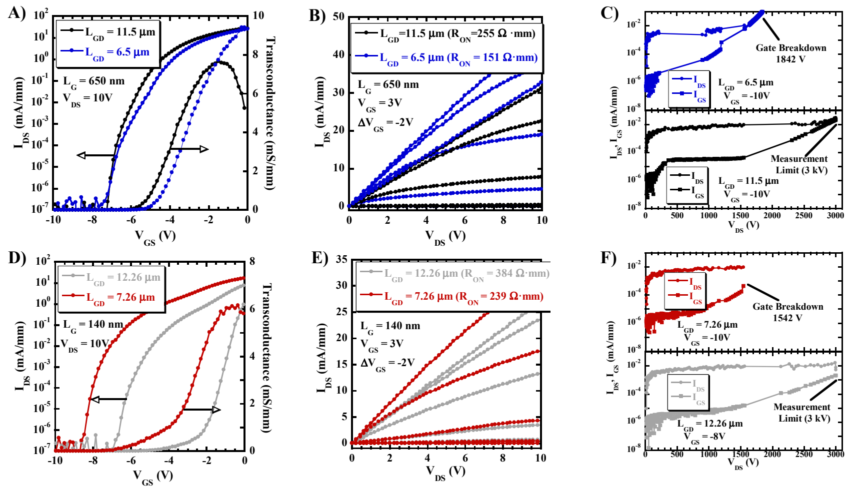

Figure 3 – Standard IV characteristics for optical gate (A-C) and Scaled Gamma Gate (D-F) MOSFETs with LGD = 11.5 µm (black), 6.5 µm (blue), 12.26 µm (gray) and 7.26 µm (red)

2016 paper analyzing the $R_{on}Q_G$ performance of a GaN vertical device [5].

DEVICE FABRICATION

A 50 nm Si doped β-Ga_2O_3 channel layer was homoepitaxially grown on a Fe doped (010) substrate by ozone molecular beam epitaxy (MBE) targeting $1.0\text{x}10^{18}$ cm^{-3} carrier concentration. Micro Van der Pauw Hall measurements indicated an achieved carrier concentration of $8.0\text{x}10^{17}$ cm^{-3}, a mobility (µ) of 78 cm^2/V·s, and a sheet resistance of 20 kΩ/□. Device fabrication began with mesa isolation using a high-power BCl_3/Cl_2 ICP etch. Contact to the active layer was achieved with a Ti/Al/Ni/Au metal stack deposited by electron beam metal evaporation followed by a 470 ºC anneal in N_2 ambient for 2 minutes. 20 nm of Al_2O_3 gate dielectric was deposited via plasma-enhanced atomic layer deposition (PEALD).

Optical I-gate contacts were defined on half of the sample via optical stepper lithography followed by Ni/Au metal evaporation. Scaled gamma-gates were defined on the remaining half via electron-beam lithography followed by Ni/Au metal evaporation. Interconnect metal was defined via stepper lithography followed by Ti/Au metal evaporation. Device cross-sections for each gate design can be seen in Figures 1 A and B.

DEVICE CHARACTERIZATION

Gate capacitance was collected as a function of gate voltage at a frequency of 1 MHz, and can be seen for the various device types in Figures 2 A and B. Integration over the collected gate voltage range produces the experimentally extracted Q_{GS} of .0014/.0011 and .00082/.00078 nC for the optical and e-beam gate devices respectively. Q_{GD} is calculated assuming maximum depletion of the

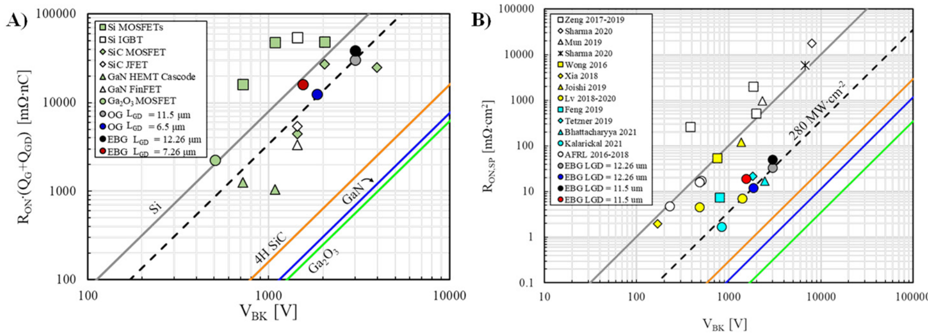

Figure 4 – $R_{ON}Q_G$ (A) and PFOM (B) benchmarking of these devices versus state of the art technology, assuming 3000 V breakdown

entire L_{GD}, Using the equation $Q = qN_DAT$. This provides a conservative representation of the total gate charge for these devices when $Q_G = Q_{GS} + Q_{GD}$ of .0060/.0041 nC and .0050/.0034 nC for optical and EBL gate devices respectively. Standard DC I-V device characterization was performed and is shown in Figure 3(A-F). Transfer data is shown in Figures 3 A and D. Good on/off ratio of $>10^8$ was achieved for all devices reported. Transconductance (G_M) of 7.5/9.5 and 6.0/6.0 mS/mm was observed for the optical and e-beam gate devices respectively. IV curves are shown for the various devices in Figures 3 B and E. R_{ON} of 255/151 and 384/239 Ω·mm was observed for the optical and e-beam gate devices respectively. Additionally, shown in Figures 3 C and F are breakdown measurements for the various device types. Breakdown voltages of 1842/3000 and 1542/3000 were achieved in Fluorinert for the optical and e-beam ate devices respectively. It is important to note that 3000 V is the measurement limit of the Tesla system used for these measurements. Thus, performance of the devices reported is likely underestimated. Finally, Figure 4 shows $R_{ON}Q_G$ (A) and PFOM (B) benchmarking of these devices versus state of the art technology, assuming 3000 V breakdown.

REFERENCES

[1] Chabak et. al., *Electron Device Letters*, 2018

[2] Kalarickal et. al., *Electron Device Letters*, 2021

[3] Bhattacharyya et. al., *Electron Device Letters*, 2021

[4] Sharma et. al., *Electron Device Letters*, 2020

[5] Zhang et. al., *Electron Device Letters*, 2019

ACRONYMS

MOSFET: metal-oxide-semiconductor field-effect transistor

BGO: β-Ga_2O_3

FOM: Figure of Merit

EBL: Electron Beam Lithography

RF: radio frequency

DC: direct current

MBE: molecular beam epitaxy

ICP: inductively coupled plasma

RIE: reactive ion etch

PEALD: plasma enhanced atomic layer deposition