CHIPS Act and its Impact on the Compound Semiconductor Industry

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Abstract

SEMI, in their 50+ years of operation, has been a trade organization supporting the semiconductor manufacturing industry with a strong membership population consisting of materials and equipment suppliers from its onset. In the mid 90's, membership jumped and SEMI broadened their scope to include member companies from across the semiconductor manufacturing supply chain, such as IDMs (integrated device manufacturers), foundries (outsource fabrication service suppliers), and EDA (electronic design automation) suppliers. We have not deviated from our base, but have added membership from across the supply chain recognizing the increasing complexity of the microelectronics ecosystem and the increasing demand for co-design and cross-collaboration of the various semiconductor disciplines at the earliest stages of development.

The semiconductor industry has experienced various inflection points over the last several decades, but perhaps none so disruptive as the present. We will look into how the semiconductor industry in general has captured the attention of the person on the street and how the industry disruptions will lead to opportunities for compound semiconductors. The U.S. CHIPS and Science Act will accelerate More than Moore technologies which in turn will further enable the integration of compound semiconductors to capitalize on the unique properties of these materials. Breakthrough opportunities will emerge with the emerging technologies developed in the Microelectronics Commons as well as the priorities of the National Semiconductor Technology Center (NSTC) and closely coupled National Advanced Packaging Manufacturing Program (NAPMP) in the CHIPS Act R&D office. A rapid focus on those technologies essential to U.S. market leadership will ensue. We will examine the emerging priorities within the CHIPS Act programs and discuss the critical role compound semiconductors play in the leap ahead technologies as well as the potential supply chain vulnerabilities that need to be addressed.

INTRODUCTION

As the semiconductor industry prepared to navigate a dramatic change to the traditional linear shrink roadmap that had affirmed Moore's Law for the last 40 years, the COVID pandemic hit. Most people, companies, and countries were caught off guard and ill-prepared. In a rush to save lives, medical professionals experienced the first supply chain bottlenecks causing shortages of personal protection equipment, a surge in demand for medical electronics such as ventilators, and depletion of testing equipment consumables. But this was only the first wave of supply chain disruptions. As the efficacy of testing and treatment methods improved, and new vaccines developed, the rippling effect would begin to affect society in other ways. Medical device shortages arose due to unavailability of electronic components in assembly, lack of domestic supplies, automotive assembly line stoppages due to semiconductor device shortages, and semiconductor equipment manufacturing delays due to "chip" shortages. Given the ubiquitous nature of semiconductor devices in our daily lives, the average person on the street started to realize how important these so-called chips were in life as we know it. So did awareness rise at the national level, and the reality of a vulnerable supply chain and its potential deleterious effect on safety and national security moved the U.S. government to action.

Semiconductor supply chain resiliency and applications that depend upon microelectronics technology leadership rapidly became a priority of the U.S. administration and governments around the world. SEMI member companies, partnering with the SEMI Advocacy team engaged with the U.S. Government to emphasize the importance of a holistic approach to developing domestic manufacturing of semiconductors critical to U.S. competitiveness and national security. As the wording developed in the House bill in the second half of 2021, the SEMI Advocacy team worked on Capitol Hill to ensure equipment and materials suppliers were eligible for the grant bill (Manufacturing Incentives plan). Emphasizing that the materials suppliers, for example, were vitally important since these facilities would need to expand to meet the U.S. capacity growth. Initial focus was on front end and the pursuit of a domestic advanced node capability. Communication continued to raise awareness for microelectronics technologies on 200mm or less wafer sizes, non-silicon technologies, legacy nodes, supply chain gaps and advanced packaging. However, a strong domestic supply chain was not the only hurdle. The availability and continuous supply of talent to fill the existing job openings and widening gap expected as a result of federal investment was highlighted. The workforce development challenge was a topic presented to the U.S. House Science Subcommittee on Research and Technology among others. Comprehensively, the House bill set the stage for the final legislation of the CHIPS and Science Act of 2022.

The CHIPS Act of 2022 has no language in the bill specifying any particular material other than the word "semiconductor." The key to compound semiconductor development as it relates to the U.S. CHIPS Act lies in scale-up of manufacturing operations through the incentives program, heterogeneous integration opportunities, and in the growth of application markets critical to U.S. technology leadership and national security. The U.S. CHIPS Act comprehensively represents a 50-billion-dollar federal investment to create helpful incentives to produce semiconductor for and in America. The two appropriations categories are the $39B Manufacturing Incentives Program and the $11B R&D and Workforce Development Program. The CHIPS R&D office responsible for the $11B investment include cross-department collaboration and initiatives such as the Microelectronics Commons hub formation by the Department of Defense, The National Semiconductor Technology Center (NSTC), and the National Advanced Packaging Manufacturing Program (NAPMP).

The majority of discrete devices and monolithically integrated circuits are made from silicon in the microelectronics industry today. Global semiconductor capacity rose to 29.6 million wafers per month (in 200mm equivalents) in 2023.[1] Approximately, 15% of that capacity represented compound semiconductors. Process development and associated processing equipment has been dominated by compatibility with silicon as Moore's law drove critical dimensions to the nanometer scale. Driven by performance and cost, linear shrinks on silicon platforms sustained the industry for decades. That was until advanced node fab costs, lithographic reticle size limits, and the yield risk of large die sizes influenced some companies to consider integrating multiple, smaller-size chips, or chiplets. The challenges of multi-chip solutions include more interdisciplinary engineering work up front, interconnect complexity, and testing to name a few. But the advantages include IP block re-use, improved defect densities using mature node chips, and performance optimization using functional or application-specific chips. This technological trend opens the door to compound semiconductors and represents a monumental paradigm shift in the microelectronics industry. Process compatibility requirements are removed. And the exceptional properties of compound semiconductors, merged with the performance of silicon circuits, will create uniquely optimized integrated systems. III-V compounds can be incorporated for the speed and energy efficiency of integrated photonics in next generation computing. Applications in extreme environments such as in military and aerospace markets, will benefit by the incorporation of radiation tolerant and high-temperature tolerant GaN and SiC chips. Wide bandgap materials can enable higher frequency operation in 5G/6G communications. The performance characteristic of compound semiconductors and the applications that will be further enabled by those unique properties will be exemplified in successful execution of the U.S. CHIPS Act.

The CHIPS and Science Act was signed into law August 9, 2022. Shortly thereafter, the CHIPS-for-America-Strategy[2] was published emphasizing the objectives to invest in U.S. production of strategically important semiconductor chips, maintaining a secure supply, strengthening U.S. technical leadership, and growing a diverse, skilled semiconductor workforce. Fundamentally, these objectives must grow to support a sustainable and vibrant domestic industry including U.S. manufacturing, U.S. R&D, and the U.S. supply chain. At the onset, advanced logic and memory manufacturing were called out as critical topics. Members of the U.S. ecosystem from small to large companies, universities, national laboratories, and trade associations were motivated to form alliances and coalitions to begin discussion on critical applications, technologies, and work force development to meet the mission of the CHIPS Act.

One of the first actions leading to industry investment from the CHIPS Act in 2023 was the Microelectronics (ME) Commons focused on university-based development and lab-to-fab transitions of commercial technology for defense application. The Department of Defense announced in September of 2023 the award of approximately $240M to eight regional "hubs" focused on microelectronics innovation in the following areas: a) electromagnetic warfare, b) quantum technology, c) 5G and 6G wireless communications, d) artificial intelligence hardware, e) secure computing at the tactical edge of the internet of things, and f) leap ahead technologies.

The first call for projects was announced in December of 2023. The broad set of projects includes opportunities for compound semiconductor development in every category. For example, wide band gap transceiver architecture and components are called out in the 5G/6G application spotlighting SiC and GaN. The AI-hardware topic includes AI sensor fusion opening possibilities of optical sensor development (transmit and receive), photonic AI compute architectures/systems, and AI in extreme environments potentially capitalizing on the radiation hardness and high temperature tolerance of GaN and SiC. The objectives of the ME Commons are to enable the transition from laboratory to fabrication in the U.S. in support of technologies identified as critical to national security. Each hub is the center point of an extended network of commercial enterprises of various sizes and academic institutions. The extended network is expected to enable access to ≥ 200mm silicon prototyping and ≥ 100mm compound semiconductor technologies.

The CHIPS for America Research and Development Office published vision papers for the NSTC and the NAPMP in April and November 2023, respectively. The NSTC will work with federal agencies and the microelectronics community to identify critical challenges and opportunities to advance the U.S. microelectronics ecosystem, strengthen domestic manufacturing, and improve national and economic security. Technical advisors from across industry, academia, DOE

national laboratories and other federally funded R&D centers will be consulted to determine specific technology focal areas. Example technical areas include multi-chip solutions, chiplets, heterogeneous integration (HI), and EDA development for HI systems. Some technical areas emphasized by members of the U.S. ecosystem in various forums are relevant to the compound semiconductor industry including power electronics, radio-frequency, mixed signal, and analog communication and sensing applications that need non-CMOS technologies, photonics, MEMS, and bioelectronics.

Figure 1 is a conceptual diagram that estimates where the various CHIPS Act R&D initiatives exist on the technology and manufacturing readiness scale (x-axis). It is envisioned that the NSTC and ME Commons research and development activities will begin at the lower TRLs (Technology Readiness Levels) with the evolution through NSTC, the tightly coupled NAPMP, and Manufacturing USA into the higher MRLs (Manufacturing Readiness Levels). Carrying it into a sustainable domestic industrial base, private sector corporations must successfully pull manufacturing and advanced technologies into the commercial supply chain. Technology transfer must be made possible from prototype lines in the ME Commons extended network, Manufacturing USA, and the NSTC and its affiliated facilities.

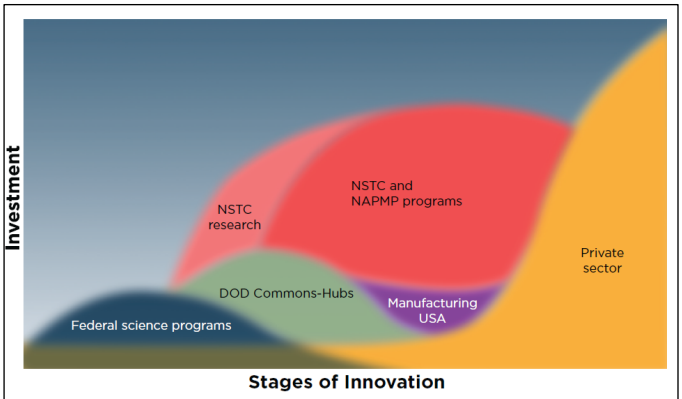

Fig. 1. A conceptual diagram of the various government programs within the CHIPS R&D office and their relative location on the continuum of innovation maturity.[3]

The NSTC vision paper mentioned advanced logic and memory which infers high performance computing (HPC) and the pursuit of leading node silicon transistor technology. The NAPMP vision paper[4], while mentioning wide-bandgap materials and photonics, leans toward HPC as well by emphasizing chip and chiplet assembly on patterned substrates using adapted CMOS equipment and processes. Addressing the processor to memory bottleneck is a clear near-term goal.[5] However, the future of computing is broader. Compute leadership includes intelligent mobile computation, or compute at the edge, such as in wearables, transportation connectivity, and other IoT applications. It includes new architectures, challenging von Neumann computing architectures, some analog, quantum, and/or bio-inspired. And it requires hardware capable of managing the enormous influx of data from the internet-of-things and the AI software algorithms necessary to accurately interpret that data.

Opportunities For The Compound Semiconductor Industry

The key to enabling compound semiconductors within the mission of the CHIPS Act are the applications considered critical to U.S. technical differentiation and national security and the trends toward heterogeneous integration.

Heterogeneous integration means different things to different people. One interpretation is the development of chiplets and 3D ICs. Chiplet technology is the disaggregation of functional groups of a larger integrated system-on-a-chip into smaller functional blocks or chiplets. A set of chiplets are assembled on a substrate, and/or stacked in 3D, and interconnected to form a multi-chip IC. Wafer-level approaches are being developed on substrates of silicon or glass, for example. Each chiplet can be optimized for cost and performance, can enable IP reuse in different devices, and can be tested so that in theory, improve the yield of the final device. Many challenges need to be tackled with respect to chiplets and further 3D advancements such as chip-to-chip physical interface and protocol standards, design PDKs and simulation tool development, and data interoperability and security. Likely, these challenges will be addressed first within silicon systems. But as standards are established, it will open the door to compound semiconductor implementation to optimize functional blocks and add new features to the disaggregated system of chips.

Another interpretation of heterogeneous integration is advanced system-in-a-package (SiP), hybrid integration, and additive manufacturing. These approaches stem from more traditional packaging and assembly technologies and historically used laminate, organic, and sometimes ceramic substrates.

CHIPS Act investment within the U.S. will be directed to strengthening the supply chain, which is not necessarily limited to North America. But just for the moment considering the capacity by region, less than 14% of the worldwide compound semiconductor capacity is in the Americas.[6] The dominant percentage of capacity exists in China at 33%. Furthermore, the majority of the compound semiconductor wafer sizes are 150 mm and 200 mm, not leading-node 300 mm. Those statistics indicate a geographical imbalance in the supply chain. However, that imbalance worsens when considering that less than 2% of the worldwide advanced packaging, assembly & test manufacturing capacity resides in the Americas.[7] Enabling the growth of compound semiconductors in key application markets through the CHIPS for America Act critically depends upon expansion of 150 mm and 200 mm fabs in North America and investment in HI and advanced packaging. Focus must be on the Manufacturing Incentive Program, establishing an NSTC that supports an

integrated network of interdisciplinary facilities, and continued diligence in contributing to the vision of the NAPMP.

Conclusions

The race to the most advanced semiconductor node, or perhaps better said, transistor design, continues to be run. The focus turns to mitigating risk in the supply chain and enabling the U.S. to compete. Advanced node or 2nm will enable various applications. Samsung laid out its 2nm mass production plan starting with mobile applications in 2025, followed by high-performance computing and automotive in successive years.[8] Advanced node is critical, but U.S. technical competitiveness and national security, both of which are CHIPS Act priorities, hinges on additional applications that include:

a) Advanced RF 5G/6G and mmwave communication systems
b) Compute at the edge
c) Next generation compute and AI architectures
d) Autonomy
e) Electrification
f) Mobility both in transportation and medical technology (such as wearables)
g) Lower energy use, particularly data centers
h) Augmented reality (AR), and
i) Environmental sustainability.

Advanced development in many of these applications is capitalizing on the unique properties of compound semiconductors. Heterogeneous solutions like non-monolithic chiplets, 3D, and advanced system integration in a package/module/board will enable the integration of optimized chips of mixed-node silicon and compound semiconductors and a vast array of sensors and transducers that collect and transmit data. U.S. compound semiconductor suppliers need to participate in and contribute to the emerging silicon-based chiplets development and weigh in on the NAPMP direction and priorities while seeking wafer capacity expansion through manufacturing incentives. With due diligence on supply chain imbalances and capabilities, heterogeneous integration (chiplets and SiP) will open up the opportunity for growth of compound semiconductors to capitalize on the high frequency, lower latency, optical, high power, energy efficiency, and enhanced reliability characteristics of this category of materials .

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Acronyms

AI: Artificial Intelligence
CMOS: Complimentary Metal-Oxide-Semiconductor
DOE: Department of Energy
EDA: Electronic Design Automation
HI: Heterogeneous Integration
HPC: High Performance Computing
IDMs: Integrated Device Manufacturers
IP: Intellectual Property
ME Commons: Microelectronics Commons
PDKs: Process Design Kits
MRL: Manufacturing Readiness Level
NSTC: National Semiconductor Technology Center
NAPMP: National Advanced Packaging Manufacturing Program
R&D: Research and Development
SiP: System in a Package
TRL: Technology Readiness Level