Defect Reduction and Yield Improvement of MIM Capacitors

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Abstract

The aim of this work is to observe and analyze strain related effects in MIM capacitor structures that lead to a degradation of fabrication yield. Our results indicate that the strain difference between the layers forming a MIM structure lead to stress-induced defects in the SiN_x insulator layer. These defects can be observed, and they become a significant yield limitation when the area / capacitance of the MIM structures is increased. Based on our technology, we propose a few process and design modifications to address the stress-related issues. Each approach was tested, and the resulting yield is presented.

INTRODUCTION

A significant portion of a monolithic microwave integrated circuit (MMIC) die is used for the metal-insulator-metal (MIM) capacitors. The number and size of MIM structures is increased in modern designs of highly efficient amplifiers. On the other hand, it is reported that integrated MIM capacitors were among 10 top causes for failure mechanisms leading to customer returns in the period 2009-2016 [1]. Therefore, the cumulative yield of all elements, and MIM capacitors in particular, should remain at the highest possible level to maintain reliable technology and low cost. We previously studied the impact of the roughness of the capacitor bottom electrode on MIM capacitor yield [2]. Such defects are the most obvious and are relatively easy to detect by optical inspection. They can be mitigated using appropriate metallization technology and an advanced MIM layer construction (see for example Fig. 5 of [1]).

From our optimization work the reasons for reduction of MIM capacitor yield were classified as follows:

- material properties and quality of the dielectric (SiN_x) used for the MIM structure,
- surface quality of the bottom electrode,
- thermal and/or mechanical stress related issues due to the sandwiched MIM structure.

In this work we present design modifications for SiN_x-based MIMs to reduce capacitor failures related to a strain in the insulator caused by thermal / mechanical stress.

TECHNOLOGICAL DETAILS

For this work the FBH standard GaN-based MMIC process flow was used [3]. During the fabrication process three layers of SiN_x with different functionality are deposited by plasma enhanced chemical vapor deposition at 325 °C. The second layer of nitride is 200 nm thick and serves as the dielectric insulator in MIMs.

Test MIM capacitors of different areas and thus capacitances were used for the yield evaluation. The capacitor breakdown voltage was used as a criterion for the determination of technology yield and its dependence on the MIM design was analyzed. The breakdown measurements were always performed on fully fabricated wafers. We used a voltage step of 1 V and a 5 V/sec ramp until breakdown failure of the MIM. The failure criterion is either physical damage or leakage current above 10 µA through the MIM structure. This current limit was kept constant for all structure types and sizes. The minimum required MIM voltage stability is 100 V for the targeted applications. Capacitors having $V_{br} < 100$ V are considered as non-functioning.

As was mentioned before, we grouped all issues leading to yield reduction by their origin. Naturally, the quality of dielectric can be controlled by the recipe and surface preparation. We optimized the surface preparation and PECVD deposition of SiN_x to reach a breakdown strength of at least 1×10^9 V/m, which means 100 V per 100 nm of SiN_x thickness. In our technology this breakdown strength transfers into an expected MIM breakdown (V_{br}) of at least 200 V, which is well above of the targeted 100 V stability. The second group of issues related to the lower MIM electrode was already tackled in our previous study [2].

DEFECTS AND THEIR ORIGIN

Despite a significant improvement of the overall yield achieved in [2] we found that reproducibility was still an issue. A significant yield degradation was detected after temperature increase in the fabrication process or die packaging and was critical for MIMs with increased area and capacitance. The average effective breakdown strength of SiN_x in MIM structures of 160×250 µm^2 was measured as about 5×10^8 V/m and was sharply decreasing with increase of structure size. At this point further observation and analysis

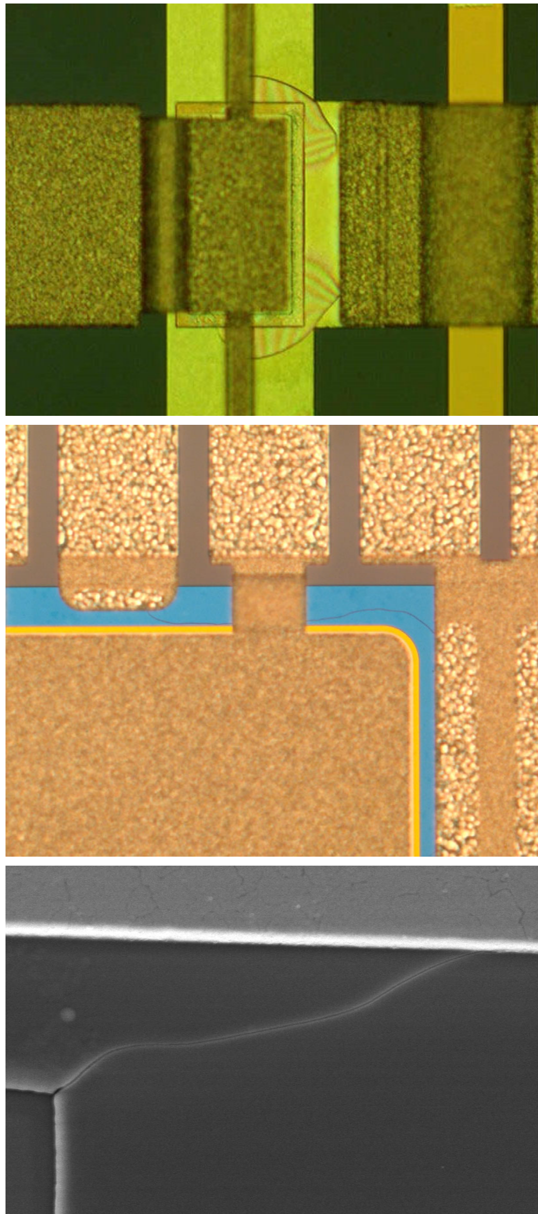


Fig. 1 Optical microscope and SEM (bottom) images show MIM structures with delamination and cracks in SiN_x deposited on the lower electrode of MIM structure.

of the defects was necessary. We noticed cracks in the SiN_x or partial delamination of the insulator from the bottom electrode in some failing parts. Cracking defects are not easy to observe since they are often located beneath the top metal electrode, but evidence of such defects can be found. Some examples of observations are shown in Fig. 1.

As can be seen from SEM image in Fig. 1 the defect propagates under the top electrode and may act as a leakage or breakdown path. The cracks usually appear during thermal treatment of the wafer in the front-end process, after backside processing, or during soldering of a die. This fact leads us to consider strains in each layer of the MIM structure, i.e. bottom and top metal electrodes and the insulator.

Since the linear temperature expansion coefficient of the metal electrodes is 3 to 4 times larger than for the SiN_x dielectric, temperature variations may produce significant mechanical stress in a SiN_x insulator confined between metal electrodes. For a 300 °C temperature increase the expected expansion difference between the metal electrodes and the SiN_x can reach 500 nm for capacitors with lateral dimension of 150 µm. Such a temperature increase may occur during front-end fabrication and die soldering as well as during device operation. Therefore, accounting for thermal stress is necessary to mitigate cracks and local delamination of the insulator in different parts of MIMs. The effect becomes more critical for large area capacitors.

By regular inspection of these defects, we identified the edges of MIM bottom electrodes as points of origin, see Fig. 2. There, the underlaying material for the 2nd SiN_x changes from metal to the first nitride. The properties of deposited nitrides are known to be dependent on the substrate material [4] and therefore thermally induced strain at the

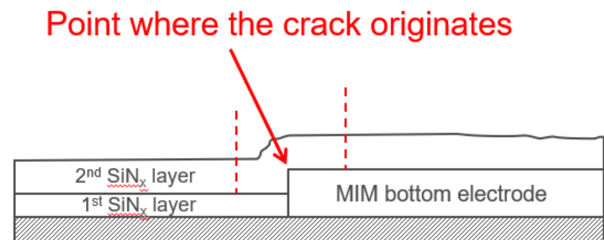


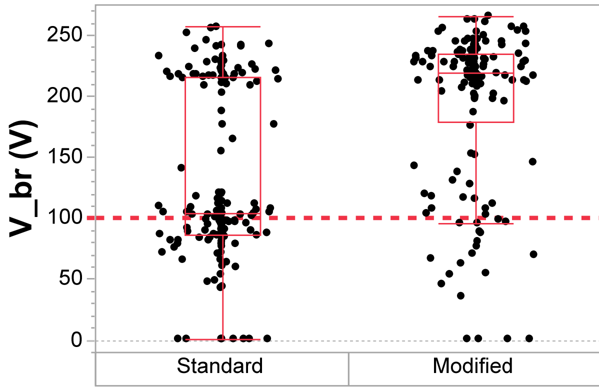
Fig. 2 Schematic cross-section of MIM structure showing the most common origin point of SiN_x cracks.

bottom electrode edge is not only triggered by the different thermal expansion coefficients of the metal and SiN_x, but also by a material discontinuity under the 2nd SiN_x layer itself.

As a result of observation and identification of the defects' root causes, we proposed and tested a few layout / process modifications for MIM capacitors. Those changes, which lead to an improved yield of capacitors are discussed in the next section.

Design and Results of Experiment

In order to eliminate the points of crack origin we removed the 2nd nitride in our capacitor in the region shown by two dashed lines in Fig. 2. This was realized by dry etching the SiN_x around the edge of the lower MIM electrode. We fabricated two variants of test capacitors with areas of 0.04 mm^2 in the same shot close to each other on standard MMIC GaN 4-inch wafers and measured V_{br}. The measurements of a total of 148 pairs of capacitors on different wafers show average (median) V_{br} of 134 V (104 V) and 194 V (219 V) for the layouts without and with SiN_x etching around the bottom electrode, respectively. The V_{br} boxplots



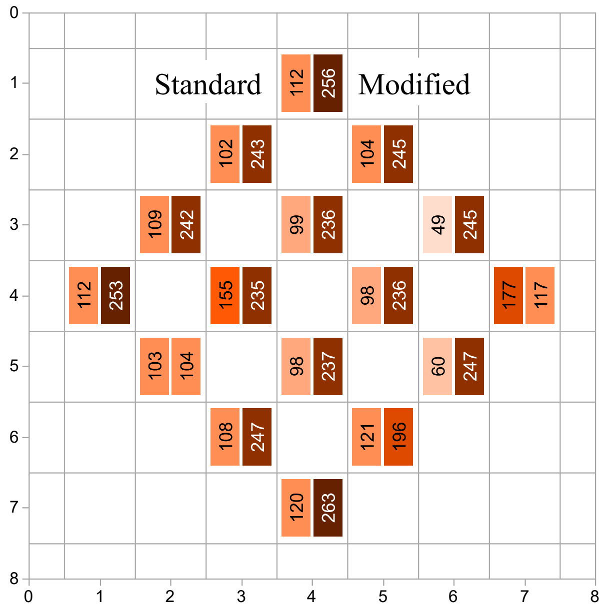


Fig. 3 Boxplot diagram (top) of V_{br} for 0.04 mm^2 MIM structures fabricated in the same exposure shot without (Standard) and with interuption of SiN_x (Modified) at the edges of bottom electrode. An example of a 4-inch wafer map (bottom) shows the results of measurements for the same types of MIM capacitors.

as well as an example of the measured V_{br} wafer distribution is shown in Fig. 3, where the direct comparison between MIM variants can be seen.

Increasing capacitance while keeping the same thickness of SiN_x requires an increase in the MIM structure area. Using the same improved design and increasing the size of the capacitor by 5 times to 0.2 mm^2 we saw a drop in average (median) value of V_{br} to 87 V (97 V), which is more than 100 V of lowering. In the second MIM design optimization run we considered the balance of stress applied to SiN_x from two metal electrodes. The stress experienced by the insulator can be minimized by fabricating both metal electrodes with comparable metallization stacks and thicknesses. In our process technology we reduce the top capacitor electrode thickness by omitting the 2nd layer, i.e. electroplated Au,

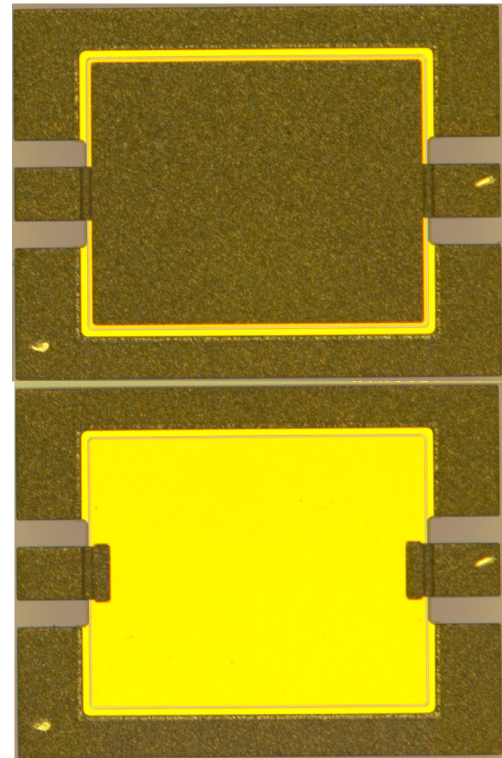


Fig. 4 Optical microscope images of MIM capacitors with top electrode formed including electroplated Au (top) and by first interconnection layer only (bottom).

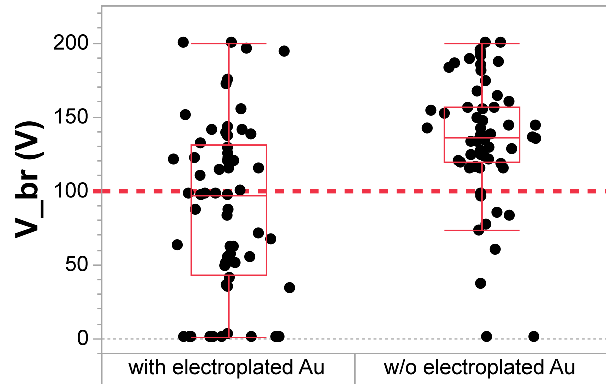


Fig. 5 Boxplot diagram of V_{br} for MIM structures (0.2 mm^2) fabricated with and without the modified top electrode in the same exposure shot.

which serves as interconnection for different parts of MMIC. The top electrode thickness is reduced by ~ 3.5 - 4.0 µm, which made it comparable to the bottom one in terms of thickness and metal stack. The microscope images of both types of MIM structures are shown in Fig. 4.

This new modification of layout improved the average (median) value of V_{br} by ~ 45-50 V as shown in Fig. 5. These results were obtained on 64 pairs of capacitors fabricated on

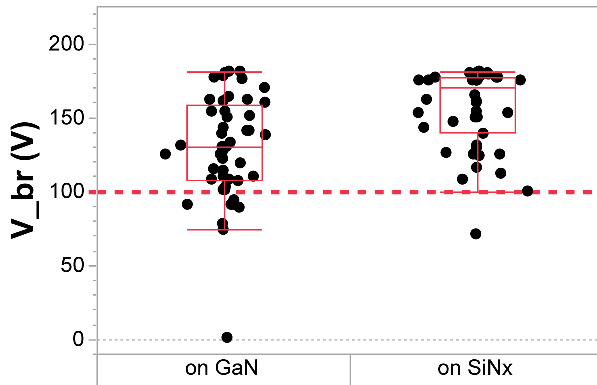


Fig. 6 Boxplot diagram of V_{br} for MIM structures (0.4 mm^2) fabricated with the bottom electrode directly on a semiconductor or on the 1st SiNx passivation layer.

the same wafers located close to each other in an exposure shot. Looking at boxplots in Fig. 5 one can see the improved distribution of the measured V_{br} values, where more than 75 % of observations are above 119 V. Nevertheless, the measured average (median) values of V_{br} 134 V (136 V) mean that the effective breakdown strength remains in the range of 6.5×10^8 V/m.

It is interesting to note that the further increase in capacitor area by 2 times to 0.4 mm^2 only slightly changes the average values of V_{br} (by ~5-6 V). This minimization of area effect indicates a more favorable stress situation in the modified structures. But the effective breakdown strength of SiN_x inside the MIM structure remains below 1×10^9 V/m, which is the breakdown strength defined for SiN_x used in MIMs.

The next iteration of yield improvement included two versions of capacitors with areas of 0.4 mm^2. In this modification, the MIM lower electrode was deposited onto the 1st SiN_x layer instead of depositing it onto GaN surface as it was in all our previous structures (see Fig. 2). Both variants of MIMs were again fabricated on a few test wafers and located close to each other in the exposure shot. The new modification leads to an increase of average (median) breakdown by 27 V (40 V) and reaches the value of 156 V (170 V) with 75 % of the measured structures having V_{br} above 140 V. This statistic represents 48 pairs of structures and boxplots of V_{br} are shown in Fig. 6. In our understanding the lower electrode helps to relax the overall stress / strain situation in capacitors. Additionally, we think that the 1st SiN_x promotes planarization of possible defects on the semiconductor surface.

After the optimization trials we fabricated test 0.4 mm^2 area MIM capacitors having all latest design improvements in a few subsequent fabrication runs. In total we analyzed breakdown of more than 600 capacitors from 30 fully processed MMIC GaN wafers. A very good statistical reproducibility was found with the average (median) values of 157 V (172 V) for the analyzed set of data. Again 75 % of the measured structures have V_{br} above 141 V.

Conclusions

In this contribution we have considered stress related defects in the dielectric of MIM capacitors. The impact of these defects on the yield and reliability of capacitors in MMIC fabrication process is shown and discussed. Several design approaches to mitigate such defects and to fabricate reliable MIM structures were presented. Our results are obtained using FBH GaN-based MMIC technology but show universal issues. Therefore, the analysis provided in this work can be used and the defect elimination approaches can be adjusted depending on the fabrication process in different process environments.

Acknowledgements

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Acronyms

FBH: Ferdinand Braun Institute for High Frequency Technique
MMIC: Microwave Monolithic Integrated Circuit
MIM: Metal-Insulator-Metal
SEM: Scanning Electron Microscopy