Time-Dependent Conduction Mechanisms in Superlattice Layers on 200 mm Engineered Substrates

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Abstract

Time-dependent conduction in epitaxial superlattice (SL) strain relief layers of GaN high electron mobility transistors (HEMTs) on 200 mm engineered substrates with a poly-AlN core were observed and analyzed. This phenomenon occurs on a timescale of 10^1 to 10^3s when the devices are operated at ~300 V, and may be enveloped by typical device operation conditions (Target 650 V). The conduction path is related to trap-assisted leakage through the SLs on the engineered substrates; separation of the charge inside the SLs forms a dipole leading to a higher electrical field across the rest of layers. This may lead to undesired effects during the operation of the devices, such as a time-dependent dynamic R_{on}. More resistive SLs will potentially reduce the impact of this phenomenon.

INTRODUCTION

Recently, GaN-based epitaxial structures for power devices have been explored on 200 mm engineered substrates with a poly-AlN core from Qromis Substrate Technology (QST®) [1] with a coefficient of thermal expansion close to that of the III-nitride epitaxial structure. A reversed stepped superlattice (RSSL) strain relief layer scheme has been demonstrated for GaN growth on QST® substrates, which induces alternative compressive and tensile stress, enabling growth of thick (7.5 µm) high quality GaN layers with low wafer bow [2], [3]. However, the electrical reliability and stability of the RSSL structure has not yet been fully assessed, which is important for enabling a manufacturable power device product. Here we report a time-dependent conduction mechanism in the RSSL when devices are biased through the substrate bias at ~-300 V. This mechanism is enveloped under typical operation conditions (devices are rated at 650 V). This time-dependent phenomenon could lead to undesired effects during the transient operation of the devices.

DEVICE STRUCTURE

The GaN high electron mobility transistor (HEMT) epitaxial structure studied here consists of a thick epitaxial stack (7.5 µm) on a 200 mm QST® substrate grown using metal organic chemical vapor deposition (MOCVD), depicted in Fig. 1(a). The RSSL is grown following an AlN nucleation layer, and includes two SL layers with different equivalent Al composition [3], which are 24% for the lower SL1 (2.4 µm) and 44% for the upper SL2 (3.7 µm), respectively, followed by a 1000 nm C-doped GaN buffer. A 200 nm UID-GaN channel is deposited following a 10 nm $Al_{0.2}Ga_{0.8}N$ barrier layer for forming the 2DEG channel; for more details of the RSSL see ref.[3]. Transfer length method (TLM) structures were fabricated on the wafer, consisting of Ohmic contacts with spacings of 10 µm, 18 µm, and 100 µm, shown in Fig. 1(b). Al-containing metal contacts penetrating from the surface of the wafer to the conductive Si (111) layer, fabricated using deep via processing were also included, shown in Fig. 1(c). The 2DEG channels of the devices were electrically isolated using nitrogen ion implantation; the Si (111) layer at the bottom of each device is electrically shorted across the wafer. These structures then enable substrate back biasing measurements, in which the conductivity between the TLM contacts is monitored as function of bias applied to the backside of the epitaxial layer stack. This provides insight

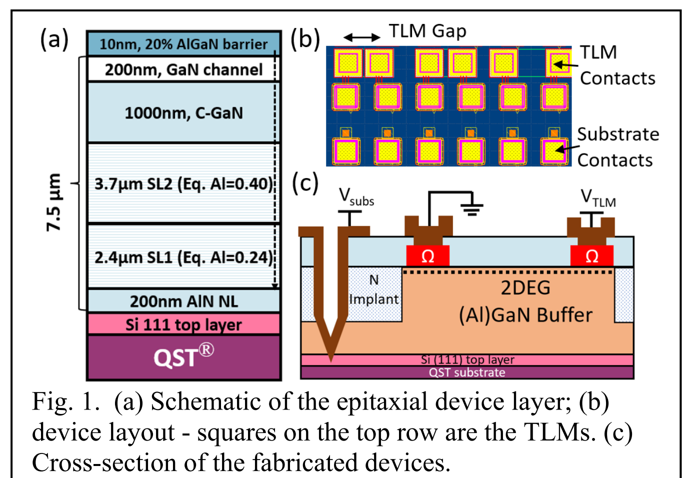

Fig. 1. (a) Schematic of the epitaxial device layer; (b) device layout - squares on the top row are the TLMs. (c) Cross-section of the fabricated devices.

into charge transport in the buffer structure. More details on the back biasing technique can be found in refs [4], [5], [6].

EXPERIMENTAL RESULTS AND DISCUSSION

Fig. 2(a) shows the current across the TLM feature with an 18 μm contact spacing with a 0.1 V applied bias, during bidirectional substrate ramps from 0 V to -900 V at the back of the epitaxial structure, with various ramp rates. The current is normalized to the initial current value at V_{sub} = 0 V. During a fast sweep rate (9.2 V/s), a hysteresis was observed similar to that which has been reported in the GaN-on-Si HEMTs[4], [5], [7]. However, there is an additional undulation observed at around V_{sub} = -300 V for slower ramp rates (1.4 V/s and 0.7 V/s). Specifically, with V_{sub} sweeping towards more negative values, the normalized current drops by ~5 % before gradually increasing until it recovers back to the saturation level. Moreover, this undulation occurs at lower voltages for the lower ramp rate of 0.7 V/s compared to 1.4 V/s.

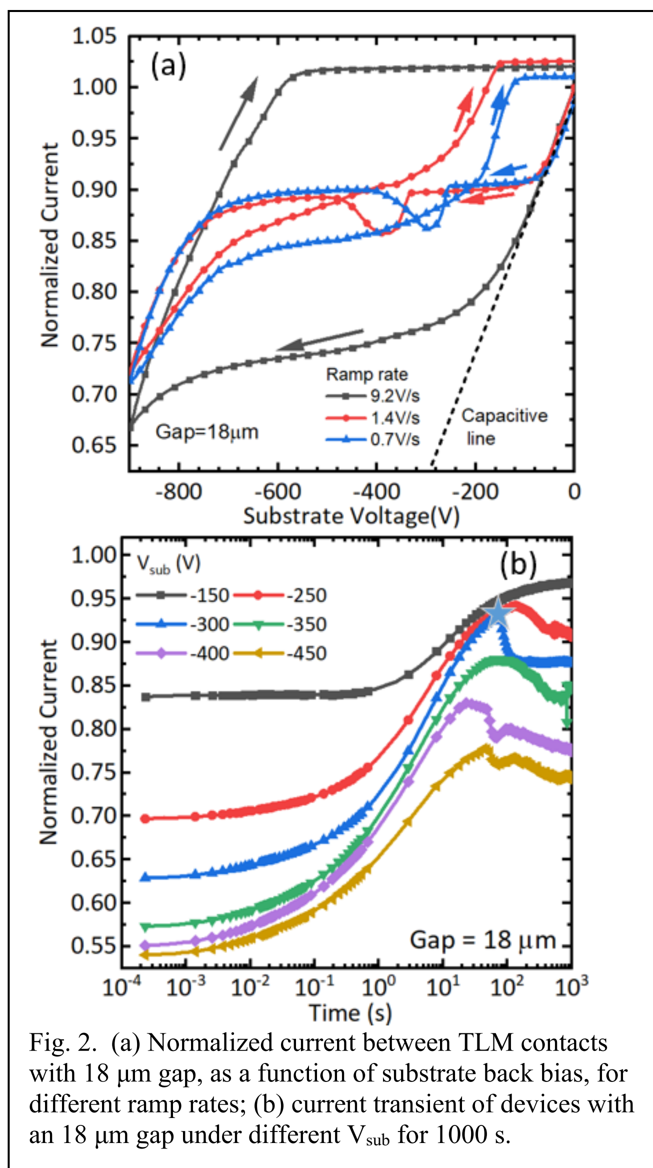

Fig. 2. (a) Normalized current between TLM contacts with 18 μm gap, as a function of substrate back bias, for different ramp rates; (b) current transient of devices with an 18 μm gap under different V_{sub} for 1000 s.

Fig. 2(b) shows the current transients on the same TLM structure at different substrate stress voltages for 1000 s. The voltage across TLM contacts is 0.1V, and the current value is normalized to the initial current value at V_{sub} = 0 V. The transient current level at the beginning points depends on V_{sub} as expected, where more negative V_{sub} values result in depletion of the 2DEG channel due to the capacitive effect of the applied negative bias at the substrate. The increase of the current over ~1 s is attributed to the band-to-band leakage through the UID GaN layer, similar to the current transient in GaN-on-Si devices. [4], [5]. A reduction in channel current occurs on a 10^1~10^3 s timescale for V_{sub} values above -250 V, corresponding to the onset of the undulation in Fig. 2(a). The largest and sharpest current reduction occurs at V_{sub} = -300 V. The onset time of the current reduction and the magnitude of the current reduction did not show an apparent dependence on the applied substrate bias.

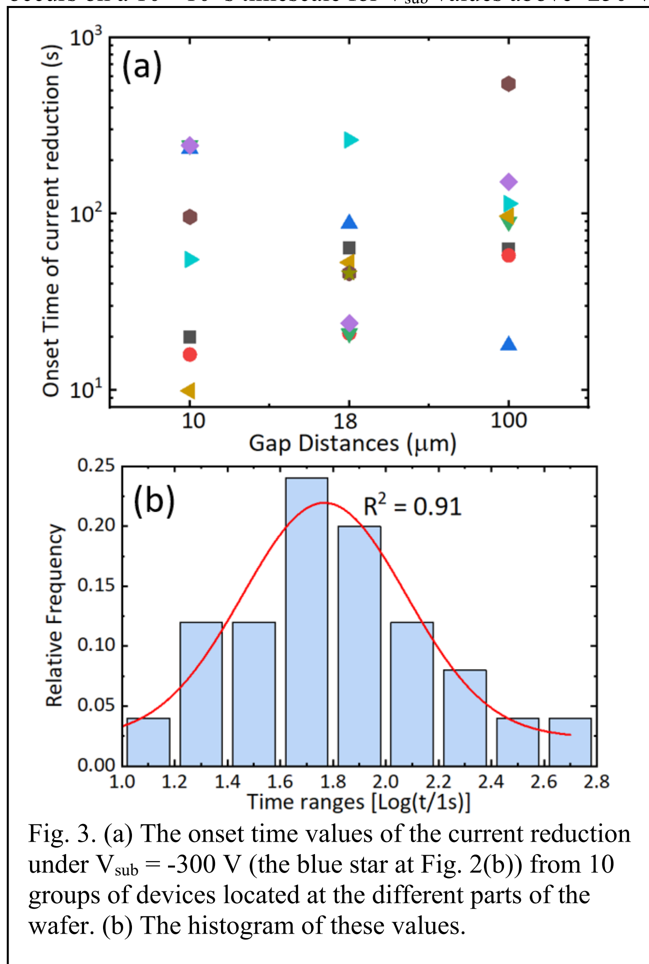

Fig. 3. (a) The onset time values of the current reduction under V_{sub} = -300 V (the blue star at Fig. 2(b)) from 10 groups of devices located at the different parts of the wafer. (b) The histogram of these values.

Fig. 3(a) shows the onset time of the current reduction under V_{sub} = - 300 V (denoted using the blue star in Fig. 2(b)) for TLM features with different contact spacings in nominally identical cells. The onset time of the current reduction of these devices is randomly distributed within the stress time range of 10^1~10^3 s with no clear relationship to the TLM contact spacing. The relative frequency (counts/total numbers) of these time values is shown as a histogram in Fig. 3(b), which follows a lognormal distribution around a central value of ~100 s.

Discussion

We make three observations on the undulation: (i) it occurs at a lower voltage under a lower sweep rate (Fig. 2(a)); (ii) it is repeatable and recoverable (results shown in Fig. 2(a) and (b) are on the same devices after fully recovering); (iii) the onset time of the undulation in the transients, is not strongly dependent on contact spacings, and follows a log-normal distribution with center around ~100s. This time-dependent, statistical nature of the current undulation coupled with its recoverable nature indicates a trap-driven conduction mechanism, rather than non-recoverable breakdown, such as via dislocations [8], [9], [10].

Fig. 4 shows representations of band diagrams of the epitaxial structure along the cutline in Fig. 1 (a) at different stages during the downward sweep of the substrate ramp. Fig. 4(a) shows the band diagram in the saturation region of the channel current during the downward sweep of the substrate ramp. A band-to-band leakage from the 2DEG through the UID-GaN (channel) layer to the GaN:C layer occurs in this region (double-headed arrow).[4]

The current undulation of the current then occurs upon application of a more negative V_{sub}. We noticed that the channel current returns to the pre-stress saturation level after the undulation (Fig. 2(a)), indicating the electric field in the UID-GaN and GaN:C layer is unchanged. However, the field distribution within the SL layers can be different. Thus, the most likely position where the conduction path generated can be assumed to be at the strain relief layers (SL1 and SL2). The undulation occurs (Fig. 2(a), (b)) most likely when part of a SL becomes conductive due to an internal leakage path that forms via trap-assisted tunneling between traps within the SLs (evidenced by the larger onset time (~100 s))[11]. Fig. 4(b) shows the band diagram when the undulation happens. The hopping of electrons causes a separation of charge inside the SLs, forming a dipole. This leads to an increase of electric field in the rest of the device's layers, which in turn causes the 2DEG to be partly depleted, manifesting as the undulation.

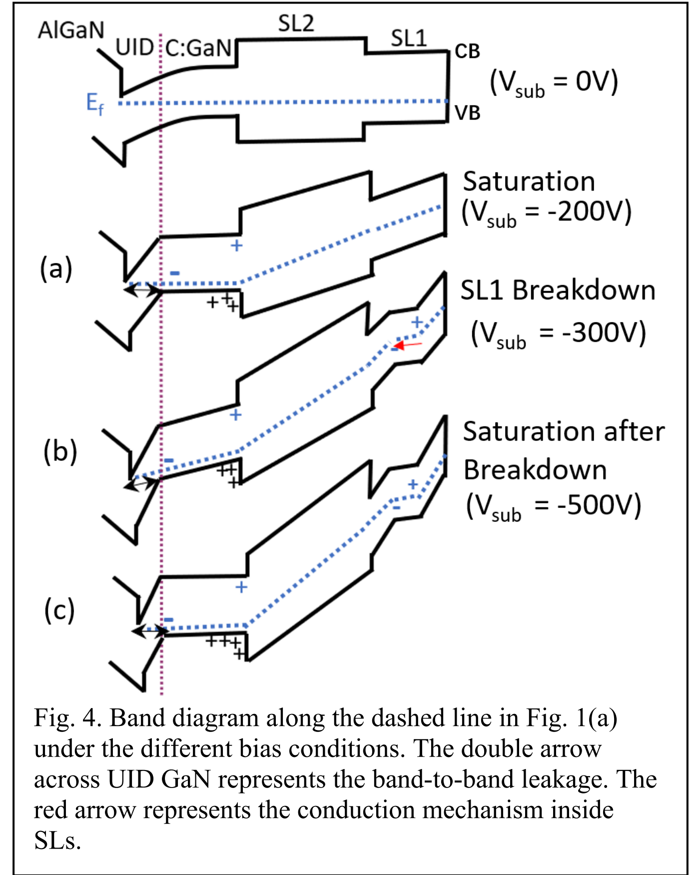

Fig. 4. Band diagram along the dashed line in Fig. 1(a) under the different bias conditions. The double arrow across UID GaN represents the band-to-band leakage. The red arrow represents the conduction mechanism inside SLs.

Fig. 4(c) demonstrates that the recovery process of the channel current after the undulation. The device recovers when charge flow through the GaN channel results in an accumulation of positive charge at the bottom of the GaN:C layer that screens the increased field in the SL, with the current then returning to its saturation value. This conduction may occur in either SL1 and/or SL2, where either becoming conductive will give rise to the change of electric field in the GaN channel layer. Fig. 4 (b) and (c) shows an example of the case that this conduction happens inside SL1.

The conduction mechanism we observed will occur when devices are operated above 300 V but will be hidden by the charge redistribution under high bias and fast ramp rate (Fig. 2(a)). The conduction path reduces the effective capacitive thickness of the SLs, possibly leading to a time-dependent dynamic R_{on} during the switching of the devices. Since the phenomenon appears to be repeatable and reversible, it seems that the local breakdown does not lead to any permanent damage, so presumably the dipole discharges when the bias is removed. A more resistive SL layer stack would potentially suppress the phenomenon.

Conclusions

We reported a conduction mechanism within the reversed stepped superlattice layers on 200 mm engineered substrates. A trap-assisted leakage inside the SLs will form when the device is operating around ~300 V, leading to a reduction of effective SLs thickness. This conduction mechanism will be enveloped by the typical devices' operation. It may result in undesired effects during the

transient operation of the devices, such as a time-dependent dynamic R_{on}. More optimization of resistance of SLs of RSSL may benefit GaN HEMTs on the engineered substrates.

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