Characterization of 1.2 kV SiC Trench MOSFETs with Buried p^+ Layers Using a Double-Pulse Circuit

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Abstract

We discuss 1.2 kV SiC trench MOSFETs with trenched p-sources and buried p+ layers (BPL) to suppress the electric field crowding phenomenon at the gate oxide. The electric fields at the gate oxide of the proposed device were successfully reduced and the breakdown voltage was increased from 1560 V to 1791 V. In addition, dynamic characteristics including rise time, fall time, and total switching loss were evaluated.

INTRODUCTION

SiC MOSFETs are gradually replacing Si IGBTs due to the superior properties of SiC such as high-temperature and high-power operation [1-5]. In particular, SiC trench MOSFETs have an advantage of low specific on-resistance because of the absence of a JFET region [6-7]. However, SiC trench MOSFETs have a problem of high electric field crowding at the gate oxide in blocking mode [8-10]. If a high electric field is constantly applied to the trench, the concentrated electric field at gate oxide may exceed the critical electric field, leading to physical failure of the gate oxide. Therefore, studying how to distribute the electric fields at the gate oxide is necessary [11-15].

Our study aims to suppress the electric field crowding phenomenon at the gate oxide and enhance the blocking capability of 1.2 kV SiC trench MOSFETs by applying a trenched p-source and a BPL. In the case of a device with only a trenched p-source, the suppressed electric field at the gate oxide was observed through deep ionization of the p-source. However, the part without a trenched p-source is not completely shielded resulting in a relatively high electric field concentrated in a portion. The proposed structure was designed with additional implantation at the bottom of the p-base to ensure an even distribution of the electric field. The device with both trenched p-source and BPL exhibits an improved blocking capability compared to using only the trenched p-source. In addition, actual devices were fabricated and compared to the Sentaurus TCAD simulations to verify the effectiveness of the BPL. The electrical properties of the SiC trench MOSFET with trenched p-source and BPL were analyzed under static and dynamic conditions.

STRUCTURE FOR CONVENTIONAL AND PROPOSED DEVICES

Figure 1 illustrates the cross-sections of the (a) conventional and (b) proposed structures for 1.2 kV SiC trench MOSFETs. The process flow for implantation of the conventional structure is as follows. First, implantation of the p-base and n-source is performed on a 4H-SiC epi-layer. Subsequently, a hard mask is deposited for p-source implantation, followed by Aluminum implantation after etching the SiC. For the proposed device, Aluminum implantation for BPL is carried out before the formation of trenched p-source. The BPL is designed with single-energy Aluminum implantation. Each active cell comprises a ladder-type layout to reduce the cell pitch. Consequently, weak spots in the gate oxide are generated due to the octagonal patterns in each p-source in Fig. 2. The proposed device is designed with striped shapes of BPL to effectively protect the trenched gate.

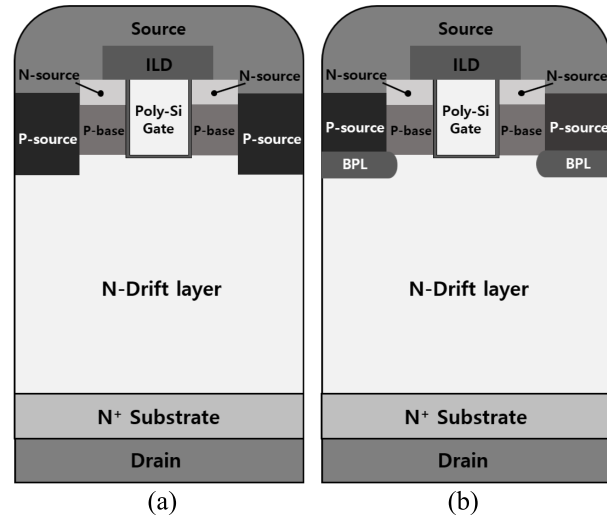

Fig. 1. Structure of (a) conventional and (b) proposed 1.2 kV SiC trench MOSFETs.

ANALYSIS OF STATIC CHARACTERISTICS

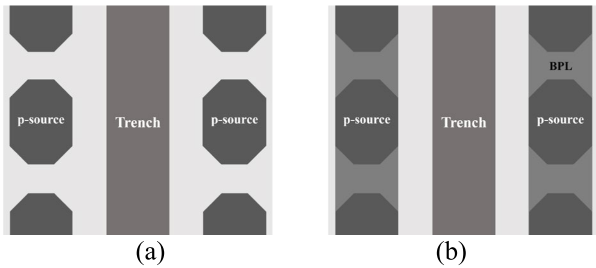

Fig. 2. Layout of (a) conventional and (b) proposed 1.2 kV SiC trench MOSFETs.

The electric field distributions of (a) conventional and (b) proposed devices at the rated voltage are presented in Fig. 3. The highest electric fields in both structures are concentrated at the bottom of the trench. However, a significantly suppressed electric field at the bottom of the trench is observed in the 1.2 kV SiC trench MOSFET with trenched p-source and BPL compared to the conventional structure. Figure 4 shows the electric field graphs along the A-A' line, which is 0-15 μm from poly-Si gate at the rated voltage. At a V_{DS} of 1.2 kV, the maximum electric field values for conventional and proposed devices are 4.2 and 3.7 MV/cm. The expected reduced electric field at the gate oxide of proposed device was seen in numerical simulations.

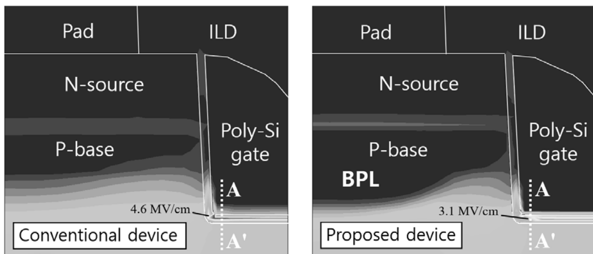

Fig. 3. Comparison of electric field distributions of conventional and proposed 1.2 kV SiC trench MOSFETs at the rated voltage.

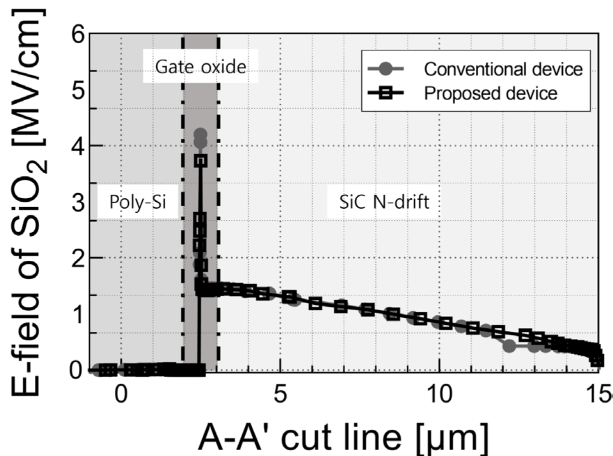

Fig. 4. Electric field graphs along the A-A' line of conventional and proposed 1.2 kV SiC trench MOSFETs at the rated voltage.

The measured conduction and blocking characteristics of fabricated SiC trench MOSFETs with trenched p-source and BPL are shown in Figs. 5 and 6. The conventional device exhibits higher drain current (I_D) due to a lower resistance in the JFET region. Furthermore, the proposed device achieves a higher BV owing to a wider depletion region resulting from the trenched p-source and BPL.

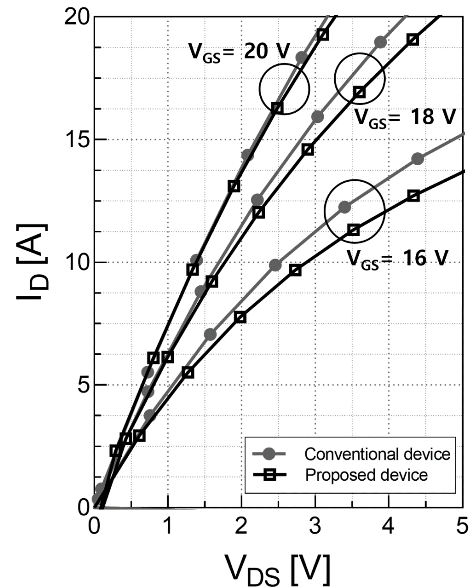

Fig. 5. I_D-V_{DS} curves for conventional and proposed devices.

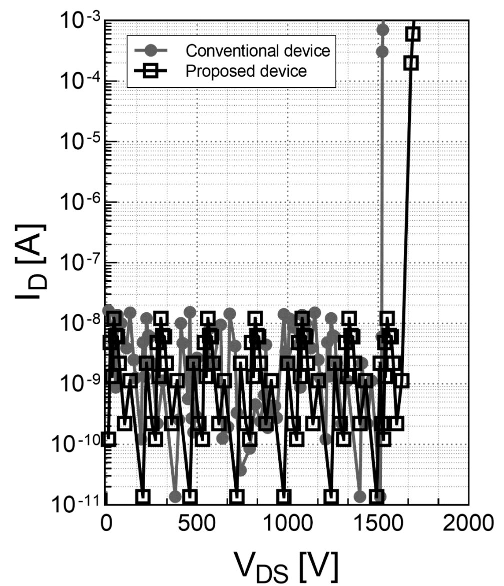

Fig. 6. BV curves for conventional and proposed devices.

The extracted $R_{on,sp}$, V_T, and BV of the conventional and proposed devices are summarized in Table I. The $R_{on,sp}$ was calculated at 18 V of V_{GS}, and the BV was extracted at 1 mA of drain current. The proposed device exhibits a slightly

higher $R_{on,sp}$ due to the increase in V_T. However, the BV increased from 1560 to 1791 V. The device using the trenched p-source and BPL has an 8% higher $R_{on,sp}$ compared to the conventional device. On the other hand, the proposed device has a 15% increased BV. It has been confirmed that the percent increase of BV from conventional device to proposed device exceeds the percent increase of $R_{on,sp}$ and V_T.

TABLE I
COMPARISON OF $R_{ON,SP}$ AND V_T, BV CHARACTERISTICS OF CONVENTIONAL AND PROPOSED STRUCTURES

Characteristics	Conventional		Proposed	
	Measurement	Simulation	Measurement	Simulation
$R_{on,sp}$ [mΩ-cm^2]	5.0	5.4	5.4	5.7
V_T [V]	5.3	4.7	5.4	4.7
BV [V]	1560	1317	1791	1418

ANALYSIS OF DYNAMIC CHARACTERISTICS

The dynamic characteristics of the devices were analyzed through a double-pulse test measurement. Two gate pulses were applied to a DUT for a brief period to measure the switching characteristics and behavioral stability of the device. The measurement conditions were as follows. An 800 V drain voltage (V_{DD}) was applied with a pulsed gate voltage (V_G) ranging from 0 to 18 V. The circuit consisted of a 120 μH inductance (L) and a 22 Ω gate resistance.

Figure 7 illustrates a circuit for double-pulse testing and Fig. 8 shows waveforms during turned-on and turned-off situations for the conventional and proposed devices. The dashed line in Fig. 7 represents the graph of the conventional device, while the solid line indicates the proposed device. Both devices showed almost identical waveforms, indicating that the use of BPL does not lead to a deterioration of the switching characteristics. The maximum drain current of the conventional device when the device changes from turn-off to turn-on is higher compared to the proposed device due to the smaller $R_{on,sp}$ and V_T. The turn-on and turn-off characteristics of the device are summarized in Table II. It has been confirmed that the addition of BPL has a negligible effect on the switching properties of device.

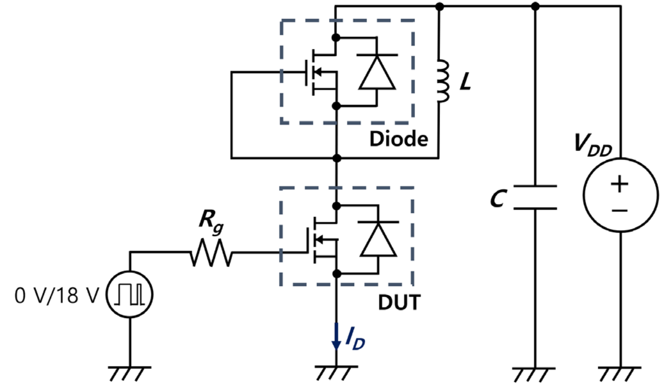

Fig. 7. Circuit for double pulse test.

TABLE II
SWITCHING CHARACTERISTICS

Extract List (V_{DD}= 800 V, V_{GS}= 0/18 V, I_D= 10 A, R_G= 0 Ω)	Conventional	Proposed
Turn-On Delay Time ($t_{d(ON)}$)	16.5 ns	23.0 ns
Rise Time (t_r)	17.6 ns	15.6 ns
Turn-Off Delay Time ($t_{d(OFF)}$)	32.8 ns	26.9 ns
Fall Time (t_f)	23.7 ns	21.5 ns
Turn-On Switching Loss (E_{ON})	256 μJ	278 μJ
Turn-Off Switching Loss (E_{OFF})	58 μJ	53 μJ
Total Switching Loss (E_{tot})	314 μJ	331 μJ

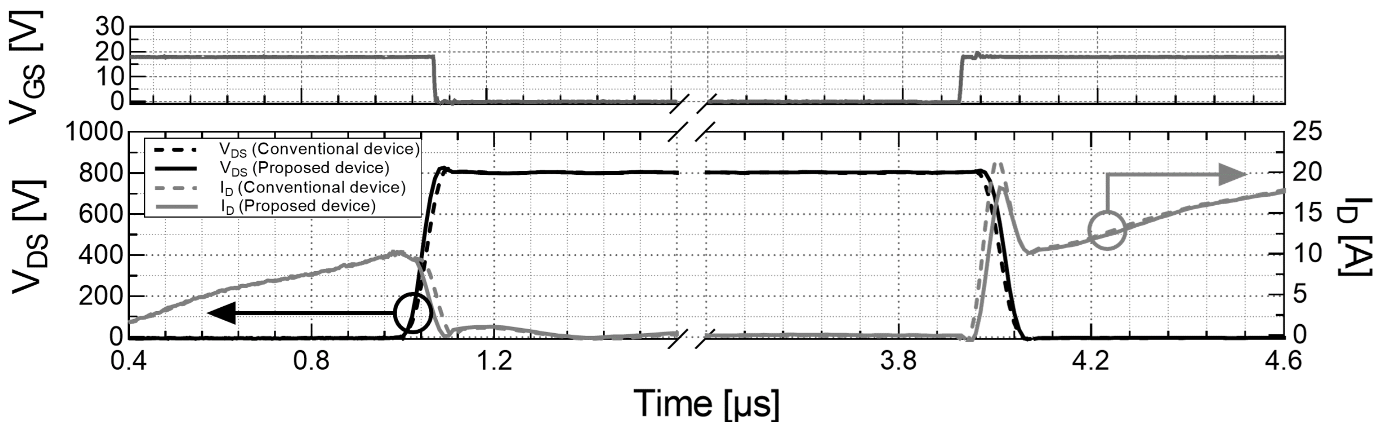

Fig. 8. Turn-off and turn-on characteristics of the conventional and proposed devices.

CONCLUSIONS

In this paper, a device with a trenched p-source and BPL was designed to disperse the high electric field at the gate oxide of a 1.2 kV SiC trench MOSFET. Depletion expanded from the BPL protects the trenched gate, so the BV is increased by 15%. In addition, we conducted double-pulse testing to evaluate the dynamic characteristics. It was confirmed that the proposed device exhibited almost identical switching power loss compared to the conventional device.

REFERENCES

[1] D. Han, J. Noppakunkajorn, and B. Sarlioglu, IEEE Trans. Veh. Technol. 63, 3001 (2014)

[2] C. Persson, U. Lindefelt, and B. E. Sernelius, J. Appl. Phys. 86, 4419 (1999)

[3] J. B. Casady, and R. W. Johnson, Solid State Electron. 39, 1409 (1996)

[4] J. Wei, M. Zhang, H. Jiang, C. Cheng, and K. J. Chen, IEEE Electron Device Lett. 37, 1458 (2016)

[5] Q. Song, S. Yang, G. Tang, C. Han, Y. Zhang, X. Tang, Y. Zhang, and Y. Zhang, IEEE Electron Device Lett. 37, 463 (2016)

[6] F. Boige, F. Richardeau, S. Lefebvre, G. Guibaud, and A. Bourennane, Microelectron. Reliab. 88, 598 (2018)

[7] M. Chaturvedi, S. Dimitrijev, D. Haasmann, H. A. Moghadam, P. Pande, and U. Jadli, IEEE Trans. Electron Devices 69, 6225 (2022)

[8] Y. Park, H. Yoon, C. Kim, G. Kim, G. Kang, O. Seok, and H. W. Ha, Jpn. J. Appl. Phys. 62, 011001 (2003)

[9] M. Sampath, D. Morisette, and J. A. Cooper, Key Eng. Mater. 946, 95 (2023)

[10] O. Seok, I. H. Kang, J. H. Moon, H. W. Kim, M. W. Ha, and W. Bahng, Microelectron. Eng. 225, 11280 (2020)

[11] Z. Guo, Z. He, F. Wang, J. Wu, Z. Yang, Z. Fan, and F. Yang, IEEE Trans. Electron Devices 69, 8 (2022)

[12] C. H. Yu, M. T. Bao, Y. Wang, H. M. Guo, Y. C. Han, and H. F. Hu, IEEE Trans. Device Mater. Reliab. 22, 476 (2023)

[13] K. Tiam, A. Hallen, H. Qi, S. Ma, X. Fei, A. Zhang, and W. Liu, IEEE Trans. Electron Devices 66, 2307 (2019)

[14] J. Wei, S. Liu, H. Tong, X. Zhang, W. Sun, and A. Q. Huang, IEEE Trans. Electron Devices 67, 5593 (2020)

[15] J. Wang and Z. Jiang, IET Power Electron. 13, 445 (2020)

ACRONYMS

BPL: Buried p^+ layer
BV: Breakdown Voltage
DUT: Device under test
IGBT: Insulated Gate Bipolar Transistor
MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor
$R_{on,sp}$: Specific on-resistance
SiC: Silicon Carbide
V_T: Threshold Voltage
WBG: Wide Bandgap