Sonic Lift-off (SLO) to Enable Substrate Reuse of Bulk GaN and SiC Substrates

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Abstract

The cost of manufacturing wide bandgap (WBG) devices is limiting an even more rapid adoption of next generation devices. Sonic Lift-off (SLO) technology offers a novel pathway to reduce such costs by separating a thin layer from a host substrate, leaving the substrate wafer available for reuse. In addition, the electrical and thermal performance of the devices benefits from the reduced thickness of the total device stack. In this work, thin layers of SiC (68.1±7.6μm) and bulk GaN (22.3±3.2μm) were acoustically separated demonstrating the potential of SLO to reduce manufacturing cost and substrate material waste while improving device performance.

INTRODUCTION

While today's power semiconductor device market is still dominated by Si-based electronics, WBG materials including SiC and GaN are making their debut for efficient power switching devices and are growing rapidly at 36% CAGR from $1.5B in 2020 to $5B in 2025 gaining more and more share in the power device market [1],[2]. The WBG device market growth is driven by mobility, clean electrification, and communication applications. WBG device manufacturers are looking for solutions to lower the cost of WBG devices to capitalize on the superior performance of WBG materials in terms of higher voltage and frequency operation, lower switching losses, and higher thermal load capability compared to Silicon devices.

Despite great performance advantages of compound semiconductor-based chips, persistently high substrate material costs will continue to restrict the more rapid deployment of advanced device manufacturing. This is because materials such as GaN, SiC, and others can cost several hundred times more per wafer when compared to Silicon. Furthermore, conventional manufacturing processes are very wasteful of substrate material, often wasting 95% or more of this precious material.

Today's standard manufacturing processes for vertical WBG-based devices typically require thinned devices, achieved by mechanical backgrinding, where most of the substrate material is wasted. Substrate materials such as SiC and GaN can consume up to 50% or more of total device manufacturing costs, depending on the specific application [3]. Besides the cost, the amount of material leftover after backgrinding has a negative impact on the resistivity and thermal conductivity of the devices [4],[5].

Crystal Sonic's Sonic Lift-off (SLO) technology provides a pathway for simple, multiple wafer reuse reducing the substrate cost proportionally with the number of wafer reuses. The SLO process has previously been shown to maintain the performance of Photovoltaic devices in GaAs [6]. In addition to the cost benefit, reducing the thickness of the final device stack in GaN and SiC would improve the performance of the device in terms of lower resistivity and greater heat transport.

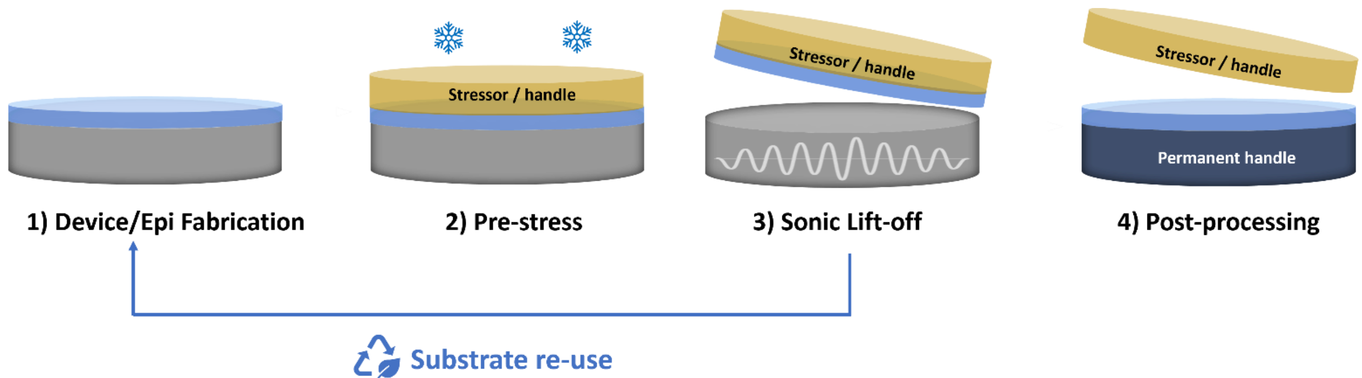

Fig. 1. Sonic Lift-off process, splitting a fabricated device or an epilayer from the substrate via acoustic energy allowing for substrate reuse with minimal processing.

EXPERIMENTAL METHODS

SLO is a novel patented technology developed at Crystal Sonic, Inc. SLO uses the combination of initiating a crack front at one side of the wafer, pre-stressing the substrate with a removable polymeric stressor to define the lift-off plane and

applying acoustic energy to successfully guide the separation of a device or epilayer from its host wafer in a controllable manner. This results in a clean lift-off of the device/epi layer from a substrate and leaves the substrate surface ready for reprocessing the next device/epi layer after no or minimal processing, as depicted in Fig. 1. In this paper, we will focus on the latest results achieved with SiC and bulk GaN.

The wafers used in this work were 50mm bulk GaN(0001) SSP with a 0.45 ± 0.1° off towards $(1\bar{1}00)$. The wafers had a thickness of 400 ± 30µm. The 50mm 4H SiC wafers used were n-type DSP with a thickness of 700 ± 25µm. Modifications on the SLO process are based on the properties of the SiC and bulk GaN wafer. A Bruker Dektak XT stylus profilometer was used to characterize the surfaces in the different wafers on 1mmx1mm areas of the samples. These experiments were performed on bare wafers to demonstrate the viability of the SLO process. Future experiments will be performed on epiwafers and devices as the starting material.

Experimental results & analysis

SLO development to date was initially developed on GaAs substrates, successfully scaling up to 100mm wafer lift-off with roughness <1µm. Here, initial SLO feasibility experiments are shown on wide bandgap materials such as SiC and bulk GaN.

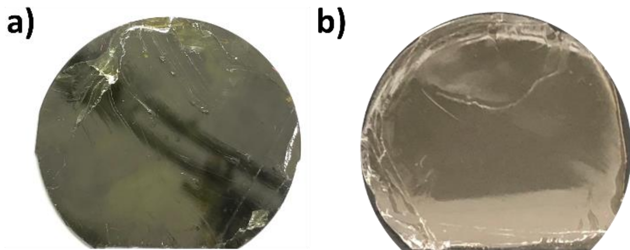

Fig. 2. Images of a) 50mm SiC and b) 50mm bulk GaN layers after Sonic Lift-Off.

Figure 2 shows images of 50mm SiC and 50mm bulk GaN samples after Sonic Lift-Off. In both cases, the lift off area was between 80%-90% of the wafer. Certain areas on the edges of the wafer were not successfully lifted off. This behavior has been witnessed in previous work by Crystal Sonic on GaAs substrates, and further fine tuning of the stress conditions can control the crack and promote its propagation to the edges of the wafer.

To analyze the surface of the substrates after SLO, areas were investigated in three different wafers for each material via profilometry. Figure 3 depicts surface profile maps of representative areas for SiC and GaN. The root mean square (RMS) roughness was measured across multiple areas. In the SiC samples the measured RMS=2.4 ± 0.9µm while in GaN was RMS=0.6 ± 0.3µm. These results indicate that the SLO process is presently better tuned for GaN than SiC. The roughness achieved in bulk GaN is considerably lower than current alternative methods to reduce the waste and cost of bulk GaN wafers. These laser-based methods require removal of >10µm of material from the damage created during the process [7],[8].

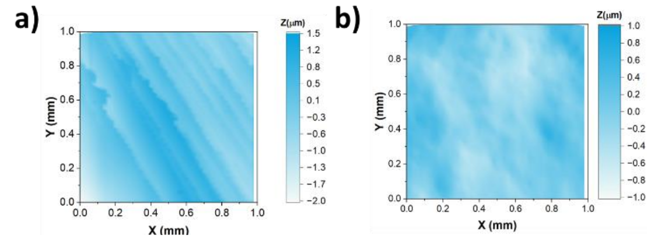

Fig. 3. Representative profile maps of SLO surfaces for a) SiC and b) bulk GaN. The RMS for SiC is 2.4 ± 0.9µm and 0.6 ± 0.3µm in bulk GaN.

The thickness of the lifted layer for each material can be tuned by modifying the process conditions such as the stressor material, thickness, among others. The SLO conditions vary for each material due to their differences in mechanical properties. The thickness of the SLO layers were analyzed for both materials. Figure 4 shows the cross section of a SiC and GaN SLO layer. The wafer thickness achieved for SiC was 68.1± 7.6µm depending on the SLO conditions. In GaN, the achieved thickness of the layers was in the range of 22.3± 3.2µm. These thin layers of SiC and GaN would substantially decrease the resistivity and increase the heat dissipation of the devices.

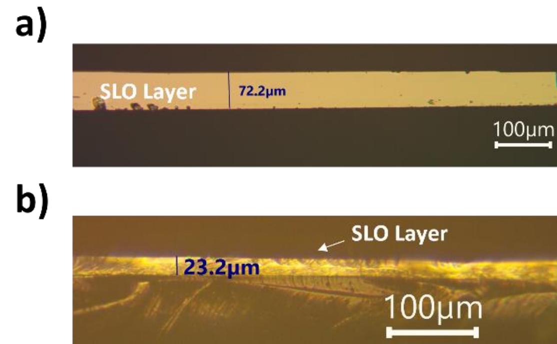

Figure 4. Cross section images of the layers after SLO in a) SiC and b) GaN wafers.

These promising results grant confidence that with further refinement, SLO can be employed in greater wafer diameter with even lower surface roughness. Future experiments will involve testing the SLO process on 100mm bulk GaN and SiC substrates, as well as devices.

Conclusions

SLO technology aims to reduce material waste during manufacturing of WBG devices and thereby drive down cost via substrate reuse. We have shown initial SLO feasibility applied into 50mm SiC and bulk GaN substrates. Thin layers with thicknesses 68.1±7.6µm and 22.3±3.2µm were acoustically separated from the original substrate. Surface

profile scans show surface roughness of 2.4±0.9µm and 0.6 ± 0.3µm for SiC and GaN, respectively. The surface roughness levels achieved for both materials suggests that the substrates could be potentially reused with a light polishing step. By removing the surface variations, the surface would be prepared for a new epitaxial growth step.

These initial results offer a promising path towards improving the thermal and electrical performance of devices while allowing substrate reusability in high quality materials such as SiC and bulk GaN.

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ACRONYMS

WBG: Wide bandgap
SLO: Sonic Lift-Off
SiC: Silicon Carbide
GaN: Gallium Nitride
GaAs: Gallium Arsenide