Key Challenges in Process Development for Future High Voltage GaN Roadmap

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Abstract

Recent development in high voltage GaN process technologies has opened up various power switching applications that Si based technologies were not able to enable. While there has been significant improvement in GaN process technology, it is still in its infancy, and there are still multiple challenges to improve its performance and reliability in order to realize the full potential of these devices. In this paper, we summarize key enablers in process technology that allowed continuous evolution of high voltage GaN devices over the past few generations. We also discuss the process technology requirements for future roadmap of this technology.

KEY PROCESS DEVELOPMENT

One of the advantages of D-mode high voltage GaN devices over E-mode is that one can use much higher 2DEG channel (n_s) as a positive threshold voltage is not required. This generally lowers specific on resistance (R_{sp}) and increases the saturation current (I_{Dmax}), which is preferred to make high performance devices. However, the higher n_S means the electric field in the channel as well as in the back-end dielectric also becomes high, which is generally challenging for various reliability issues including time-depending dielectric breakdown (TDDB) [3-4] or current collapse and dynamic R_{ON} problems [5-6].

In addition, there is effectively no holes available in the device that can compensate electron trapping and recovers the current collapse unlike p-GaN based devices [6], This requires optimization of several processes to minimize the trapping effect. In this section, we first summarize the key process modules that enable high performance and solid reliability [1, 7].

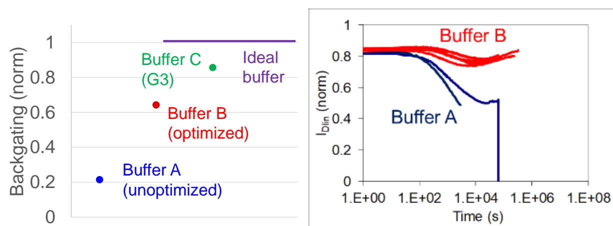

Fig 1. (Left) Backgating characteristics for 3 processes. The data is normalized to ideal capacitive buffer. The optimized process (B & C) gives reduced backgating effect. (Right) Dynamic performance and reliability of Buffer A & B under hard switching stress at 600V and 150°C. The reduced backgating (buffer B) results in improved hard switching stability and robustness.

Epi optimization

GaN epitaxial growth is one of the keys for developing a reliable high voltage GaN technology. It not only serves as a foundation to build the device, but is also a critical part of the device design and process integration. Some of the key challenges for high voltage GaN epi include high blocking voltage and reduced traps around the critical device area to minimize the current collapse. In particular, the back-gating effect has been identified to be one of the key performance metrics for high voltage devices [8]. Depending on the interface/bulk trapping and conductivity of the material, an epi stack can exhibit different back-gating behaviors [9].

We have optimized these parameters to improve the backgating characteristics (Fig 1). The latest buffer (C) is approaching the ideal capacitive behavior. As it can be seen, the improved back-gating characteristics has a significant impact on the hard switching performance, reliability, and robustness [7]. This also allows further scaling device dimensions to improve the technology.

Surface passivation

It is widely known that the surface passivation to minimize the surface states and traps is critical for controlling the current collapse [10]. This becomes even more important when scaling the device to improve R_{sp}. This is because

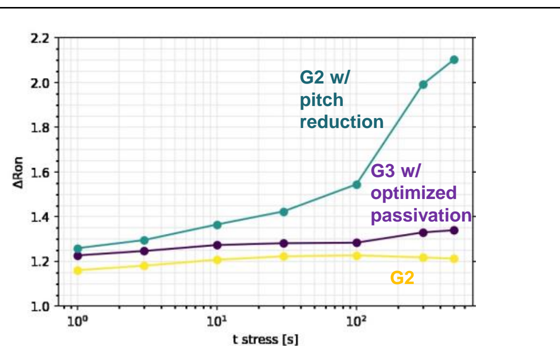

Fig 2. Dynamic R_{ON} performance of 3 processes under 560V/150°C hot carrier stress. When the device pitch is scaled, d-R_{ON} significantly increases, but with the optimized passivation, it becomes stable.

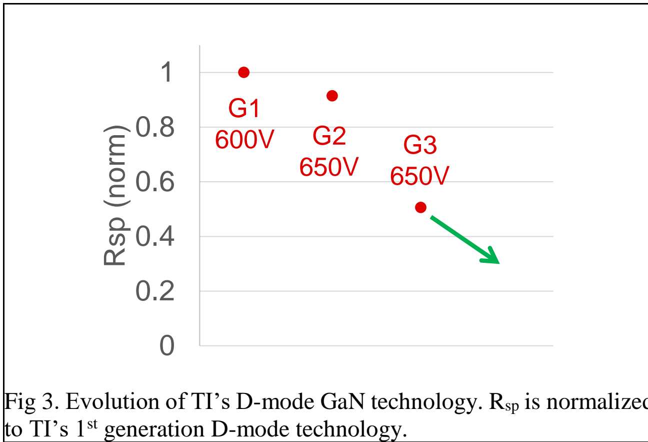

Fig 3. Evolution of TI's D-mode GaN technology. R_{sp} is normalized to TI's 1st generation D-mode technology.

scaling the device pitch inevitably increases the E-field in the channel, producing more hot carriers that can be trapped at the surface. Fig 2 shows an example of how optimized surface passivation can help reducing the device pitch. Even with the increased hot carrier injection due to the reduced device dimension, a better passivation can still make the device stable against hot carrier trapping.

CHALLENGES FOR FUTURE ROADMAP

Fig 3 shows the R_{sp} improvement of TI's D-mode high voltage GaN technology. We have improved the intrinsic R_{sp} by about 25% for each generation (the voltage rating was increased from G1 to G2, which impacted the overall R_{sp}). This has been done through various process optimization and development mentioned above.

For future nodes, although there is still room for further optimizing each process module to shrink device dimensions, we need to consider novel device architecture and integration such as multi-channel HEMT devices [11] and optimized back end.

Another key vector to improve the performance and reliability of GaN devices is co-optimization of the driver and the GaN power device (Fig 4). The integrated driver and power FET allow optimized gate control and adds critical functionalities such as over-current and over-temperature protection to improve system level reliability.

CONCLUSIONS

We have discussed key process technologies that enabled continuous scaling of high voltage GaN devices. This includes epi stack optimization, surface passivation in addition to device architecture engineering.

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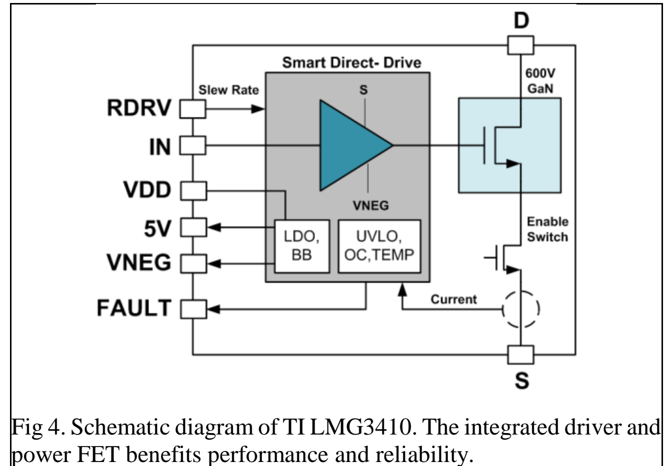

Fig 4. Schematic diagram of TI LMG3410. The integrated driver and power FET benefits performance and reliability.

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