Expanding the Scope of GaN Power Integration

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Abstract

GaN power integration technology offers an effective way to help unlock the full potential of GaN power electronics for next-generation power supplies and converters, which require high efficiency and high power density. This paper provides an overview of the current state of GaN power integration, based on the commercially available p-GaN gate HEMT platform. We focus on the development of peripheral gate driver, GaN-based complementary integrated circuits, reverse-conducting transistors, and substrate engineering for half-bridge monolithic integration. Moreover, we will illustrate the potential for expanding the scope of GaN power integration toward innovative device architectures, such as the GaN/SiC hybrid field-effect transistors (HyFETs), which harness the complementary merits of both GaN and SiC devices. Exploration of GaN-based memory devices is also included.

I. Introduction

Gallium nitride (GaN) power integration technology has made significant progress in recent years, with various GaN-based power devices and integrated circuits (ICs) being developed and commercialized [1, 2]. The planar nature of the GaN heterojunction-based high electron mobility transistor (HEMT) platform enables high-density integration. This capability can lead to increased functionality, optimized performance, and improved reliability of power electronic systems [3]. Such advancements are particularly important for applications such as compact fast chargers, high-speed drivers for light detection and ranging (LiDAR) devices, and power supplies in data centers.

Despite these advantages, several challenges need to be addressed to fully exploit the potential of GaN power integration. One major challenge is the development of GaN-based complementary metal-oxide-semiconductor (CMOS) circuits, which are crucial for achieving high energy efficiency in power electronic systems [4]. The absence of mature p-channel FETs (p-FETs) has impeded the development of GaN CMOS circuits, leading to high static power dissipation in logic circuits based on GaN [5]. Another challenge is the substrate-induced cross-talk, which limits the integration of high-side and low-side power switches in a half-bridge topology [6, 7]. Addressing these challenges effectively is essential for the widespread adoption of GaN power integration technology.

As the field of GaN power integration continues to evolve, new and innovative technologies are being developed to further enhance the performance and capabilities of GaN-based power electronic systems. One such emerging technology is the hybrid field-effect transistor (HyFET) that combines the benefits of GaN with SiC in a vertically integrated device [8]. This development paves the way toward GaN/SiC hybrid power ICs that could further improve the performance and functionality of power electronic systems. Another recent advancement is GaN-based non-volatile memory (NVM) devices, which have shown high speed, high endurance, and long retention times; these qualities make them a valuable addition to the GaN power integration ecosystem. [9]

This paper provides a broad overview of the current state of GaN power integration, focusing on the development of peripheral circuits, GaN-based CMOS technology, and substrate engineering techniques. Additionally, it explores potential advances in device architectures, offering insights into the emerging prospects of GaN power devices in the rapidly evolving field of power electronics.

II. GaN Power Integration: Current State and Challenges

2.1 GaN Peripheral Circuits for Gate Driving

Figure 1 schematically depicts a GaN power integrated circuit based on the p-GaN gate HEMT platform, which is currently the most widely used for GaN power integration. This platform offers a wide range of devices with different voltage ratings and low on-resistances. Enhancement mode (E-mode) and depletion mode (D-mode) operations can be simultaneously realized by either retaining or etching away the p-GaN cap above the channel. In addition to the high voltage (HV) transistors, low voltage (LV) devices are also available, featuring a smaller drain-to-gate distance (L_{GD}). Essential components for power ICs, such as diodes, capacitors, and resistors, can be integrated into the platform. These components include structures such as the lateral field-effect rectifier (LFER), the 2-dimensional electron gas (2DEG) resistor, and the p-GaN stack capacitor [10-12].

The development of GaN-based peripheral circuits for gate driving and sensing/protection has been a key research focus in recent years. These circuits are critical for the safe operation of GaN power transistors because p-GaN gate HEMTs are vulnerable to gate reliability issues and false turn-on due to their low threshold voltage (V_{th} < 2 V) and maximum safe operating gate voltage (V_{G_max} < 7 V). Therefore, integrating gate drivers is of great benefit for high-frequency switching, as it helps minimize the impact of parasitics and ensures safe and efficient ooperation. Figure 2 illustrates a typical integrated gate driving circuit that includes a charge pump unit for faster switching. [13]

2.2 GaN-Based CMOS Circuits

CMOS circuits are widely used in silicon-based power electronics because of their low static power dissipation and high-speed operation. However, the development of GaN-

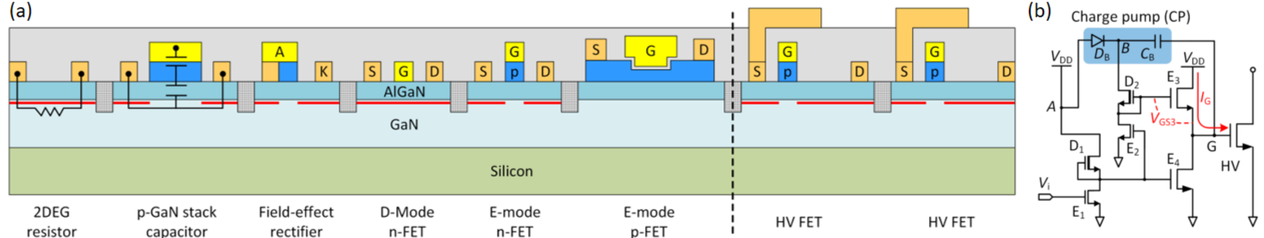

Fig. 1. (a) Power integration platform based on p-GaN gate HEMT. (b) Gate driving circuit featuring a charge pump unit.

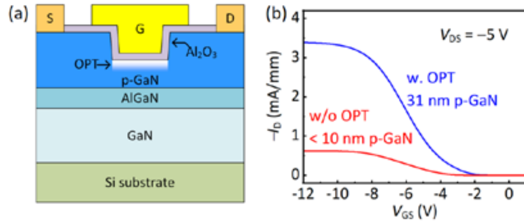

Fig. 2. (a) Cross-section schematic of an E-mode p-FET realized on the previously discussed platform, with oxygen plasma treatment. (b) Transfer characteristics of p-FETs with different gate designs.

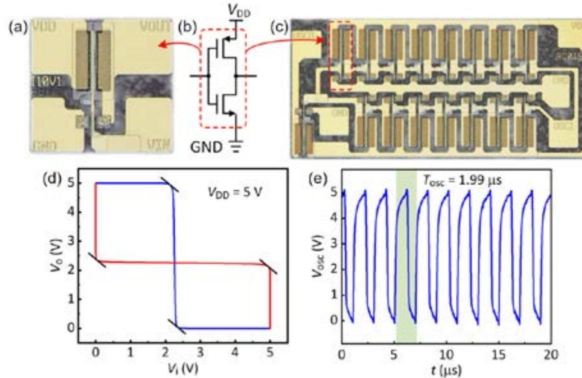

Fig. 3. (a) Photo of the integrated GaN CMOS inverter. (b) Schematic of a CMOS inverter circuit. (c) Photo of the GaN CMOS ring oscillator. (d) Cross-coupled transfer characteristics of the inverter. (e) Oscillating waveform of the ring oscillator.

based CMOS circuits has been hindered by several technical challenges, primarily the fabrication of GaN p-FETs. As a result, current GaN driver IC designs relied on directly coupled FET logic (DCFL), and GaN CMOS was absent, as depicted in Fig. 1(b). The low hole mobility in GaN materials and the difficulty of achieving effective p-doping have posed significant barriers to the development of GaN p-FETs. Nonetheless, recent research efforts have led to significant advancements in GaN p-FET fabrication, with improvements in epitaxial structures, device configurations, and ohmic contact formation [14].

In the p-GaN gate HEMT platform, the p-cap layer facilitates the integration of p-FETs. More importantly, it allows for the simultaneous realization of both HV and LV n-FETs with p-FETs. Figure 2 illustrates a p-FET formed on the p-GaN gate HEMT platform featuring a 'moderately recessed + oxygen plasma treated' gate. This configuration achieves a good balnce between E-mode operation, ON/OFF ratio, and ON-resistance [5]. The device has been instrumental in the demonstration of GaN-based CMOS logic gates and multi-

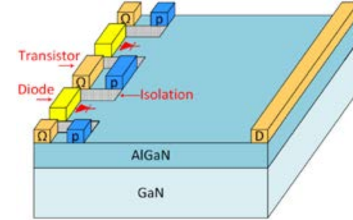

Fig. 4. GaN RC-HEMT integrating the function of a transistor and a diode. The transistors and diodes are interleaved with common access region.

stage logic integrated circuits, as shown in Fig. 3. Despite these advancements, further research is essential to enhance the performance, stability, and reliability of GaN p-FETs and GaN-based CMOS circuits [15]. Such improvements will be crucial for the adoption of GaN CMOS technology in power electronics applications.

2.3 GaN Reverse-Conducting Transistors

In some power electronics applications such as AC matrix converters, power switches are required to conduct current in both forward and reverse directions. In Si or SiC power switches, a buried body diode provides the reverse conduction at $V_{GS\text{-}OFF}$, while in GaN HEMTs, the transistor conducts a reverse current through the gated channel at $V_{GS\text{-}OFF} - V_{DS} = V_{th}$. However, the V_{th} for GaN HEMTs is typically higher than that for the Si body diode, resulting in a higher reverse turn-on voltage (V_{RT}). To mitigate this, recent research has introduced the GaN reverse-conducting HEMT (RC-HEMT), which integrates interleaved built-in Schottky barrier diodes (SBDs), as demonstrated in Fig. 4 [16].

III. Expanding the Scope of GaN Power Integration: Toward 3D and Memory Devices

3.1 Substrate Engineering for GaN Half-Bridge Integration

Monolithic integration of high-side (HS) and low-side (LS) power switches in a half-bridge topology [Fig. 5(a)] is highly desirable for high-frequency power converters because it substantially reduces parasitic inductances in the interconnects. However, substrate-induced cross-talk presents a significant challenge for the single-chip integration of GaN-on-Si power HEMTs in this configuration. This effect occurs when the common Si substrate used for GaN power HEMTs acts as an electrical conduit for both high-side and low-side transistors, leading to unwanted interactions (e.g., buffer trapping and negative back-gating) between the devices.

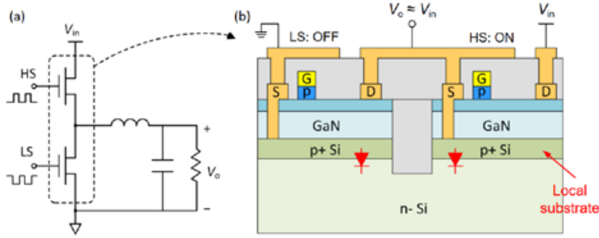

Fig. 5. GaN power integration platform on engineered bulk silicon substrate (GaN-on-EBUS).

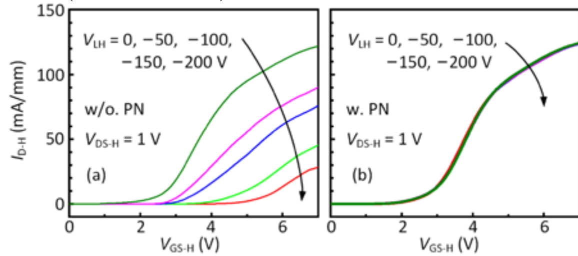

Fig. 6. (a)-(b) Experimentally measured I_D-V_{DS} curves demonstrating the cross-talk effect on the HS-transistor on a conventional platform and on the EBUS platform.

Several substrate-engineering techniques have been proposed to mitigate this issue, including the use of GaN-on-Silicon-On-Insulator (SOI) epitaxial layers and GaN-on-Electrically-Buried-Substrate (EBUS) structures [6, 7]. These methods create multiple isolated electrical substrates on a common mechanical substrate. In the GaN-on-EBUS approach (Figure 5(b)), an n-Si substrate with a p-doped layer on top is utilised. Deep trenches are etched to form isolated single GaN HEMTs. The source of each GaN HEMT is connected to the p-region on its respective island, allowing the pn diodes to block the electric field from the Si substrate, thereby eliminating the substrate-induced cross-talk effect. The effectiveness of GaN-on-EBUS in suppressing cross-talk is experimentally validated by measuring the current degradation in the HS-transistor, as depicted in Fig. 6. In traditional half-bridge integration, where the Si substrate is connected to the source of the LS-transistor, a negative back-gate voltage, V_{LH} (or the -V_{DS-L}) is constantly applied to the HS-transistor, leading to I_{D-H} degradation [Fig. 6(a)]. In contrast, in the GaN-on-EUBS platform, the current of the HS-transistor remains stable under varying V_{LH} conditions, as demonstrated in Fig. 6 (b).

3.2 GaN/SiC Hybrid Field Effect Transistor (HyFET)

Nowadays, GaN and SiC are the most prominent wide bandgap semiconductors used in power devices. On one hand, despite the high-mobility of the 2DEG channel and low terminal capacitance of lateral GaN HEMTs, these devices face several challenges. These include area inefficiency for voltage scaling, the 'dynamic R_{ON}' issue, and the lack of avalanche capability. On the other hand, even though vertical SiC MOSFETs benefit from well-developed selective pn structures (enabled by mature ion implantation and activation techniques) for voltage blocking and have established manufacturing processes, they still face the major roadblock in low channel mobility and large channel resistance. Hence, combining GaN and SiC in a hybrid device presents an opportunity to harness the complementary strengths of both lateral GaN (channel) and vertical SiC devices.

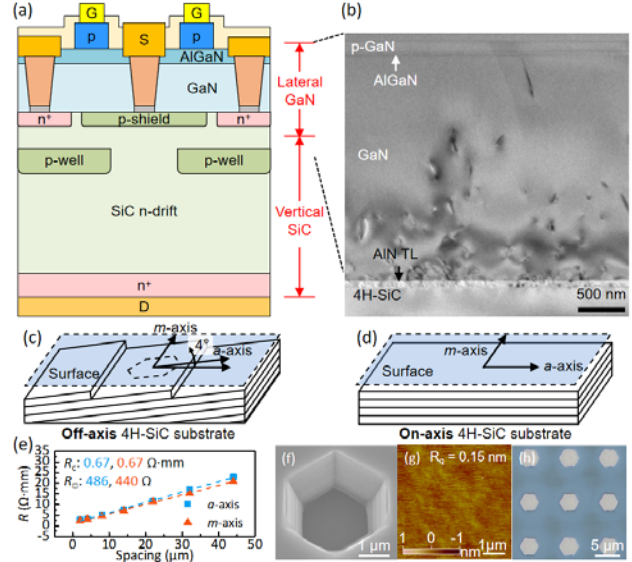

Fig. 7. (a) Cross-sectional structure of the GaN/SiC HyFET. (b) TEM image of the III-nitride epilayers. (c),(d) SiC substrates used for GaN epitaxy: (c) 4°-off-axis, (d) on-axis. (e) Sheet resistance ($R_□$) and contact resistance (R_C) of 2DEG along *a*- and *m*-axes. (d) SEM image of a TGV. (e) AFM results of the SiC surface in the TGV. (f) Photo of the Cu-filled TGVs.

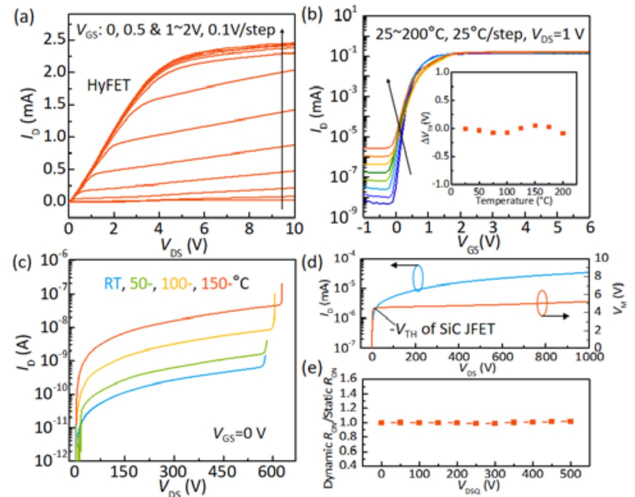

Fig. 8. Characteristics of HyFET: (a) output chracteristics, (b) temperature-dependent transfer characteristics with the inset showing the V_{TH} shift, (c) temperature-dependent off-state breakdown, (d) Voltage stressed on the GaN channel under high drain bias, (e) dynamic R_{ON}.

Recently, the first monolithic GaN/SiC HyFET was experimentally demonstrated, as shown in Fig. 7 [17]. This device utilizes a GaN heterostructure channel and a vertical SiC voltage blocking (pn junctions) and drift region to obtain low channel resistance and kV-level voltage blocking. To fabricate the device, firstly, a dual-epitaxy of SiC was performed to form a JFET structure. Second, high-quality GaN epitaxy should be grown on the SiC structure. The required substrate for vertical SiC power devices is the 4° off-

axis 4H-SiC [Fig. 7(c)], while GaN epitaxy is usually grown on on-axis 4H-SiC [Fig. 7(d)]. The anisotropic off-axis 4H-SiC substrate presents a major challenge. In our work, a two-step biaxial strain release technique has been developed [18]. When III-nitride epitaxy was grown on off-axis 4H-SiC, the strains along the *m*- and *a*-axes were designed to be primarily released at the GaN/AlN and AlN/SiC interfaces through misfit dislocations (MDs) and geometrical partial misfit dislocations (GPMDs), respectively. This method has resulted in high-quality GaN epitaxy [Fig. 7(b)] as evidenced by the small rocking curve FWHM [333/243 arcsec at (102)/(001)] and the isotropic electrical properties of the GaN 2DEG [Fig. 7(e)]. Third, the device fabrication was completed using a standard GaN HEMT process, which included through-GaN-via (TGV) etching and a Damascene-process-based in-cell interconnect, as depicted in Fig. 7(f)-(h).

The characteristics of the HyFET are plotted in Fig. 8. The device exhibits a thermally stable V_{TH} at high temperatures. As demonstrated in Fig. 8(c) , the device maintains non-destructive breakdown with a positive thermal coefficient, indicative of an avalanche process enabled by the SiC pn junctions. At a 1 kV drain bias, the voltage drop across the GaN channel is only ~5 V [Fig. 8(d)], and hence the device effectively avoids the dynamic R_{ON} issue [Fig. 8(e)].

3.3. GaN Non-Volatile Memory (NVM) on Power Platform

The wide bandgap of GaN offers a broad energy window that can accommodate deep-level traps, making it a promising material for non-volatile memory devices. Recent research has demonstrated GaN-based NVM devices that exhibit high speed, high endurance, and prolonged retention times, utilizing a p-GaN gate HEMT platform [Fig. 9] [9]. Program and erase (P/E) operations are achieved through bipolar charge injection via the p-FET channel and 2DEG back gate (BG), with charge trapping occurring at the interface deep-level states in the charge storage layer (CSL). Benefiting from highly efficient and minimally destructive drift/diffusion-based P/E processes, the proposed GaN-based NVM delivers fast operation speeds, requiring only 200-ns for P/E cycles, endurance of over 10^{10} cycles and extended retention times.

IV. Conclusions

GaN power integration technologies exhibit significant potential to revolutionize the field of power electronics. Advances in GaN power devices and integrated circuits, along with the emergence of innovative technologies like GaN/SiC hybrid field-effect transistors and GaN-based non-volatile memory devices, showcase the multitude of opportunities and advantages that GaN power integration offers.

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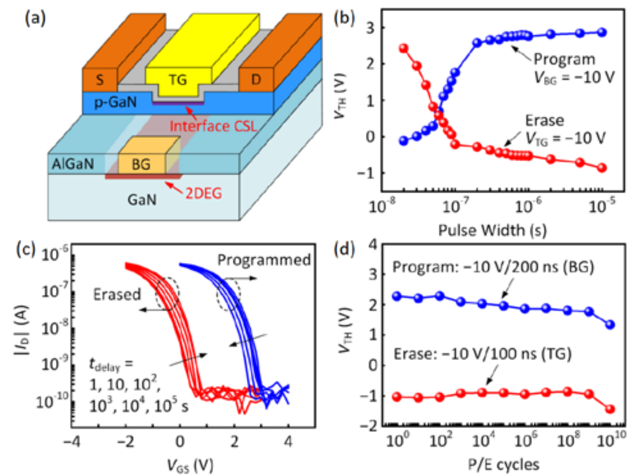

Fig. 9. (a) Schematics of the GaN-based charge trapping NVM. (b) P/E speed of the GaN-based NVM, with V_{th} measured after P/E pulses of varying widths are applied. (c) Retention characteristics, with transfer curves measured at different delay time (t_{delay}). (d) Endurance performance of the NVM, with V_{th} measured after applying different numbers of consecutive P/E pulses.