Overlapping source field plate process module for high-voltage GaN HFETs with low off state leakage currents

Houssam Halhoul*, Ralph-Stephan Unger, Frank Brunner and Oliver Hilt

Ferdinand-Braun-Institut (FBH), Leibniz-Institut für Höchstfrequenztechnik,
Gustav-Kirchhoff-Strasse 4 12489 Berlin, Germany
*email: houssam.halhoul@fbh-berlin.de, Tel. +49 30 6392 8233

***Abstract*— GaN-based high-voltage HFETs have been fabricated using single source-connected field plates. The device breakdown voltage was as high as 2370 V for 15.5 µm gate drain separation. A breakdown-voltage scaling as function of the gate-drain separation of 150 V/µm was achieved benefiting from the use of AlN as a buffer layer. The off-state leakage current associated with strain induced by the 2nd SiN_x passivation layer decreased by around one order of magnitude after releasing this strain by opening the SiN_x on top of the gate metal stripes. These openings were filled with BCB before the field plate metallization. This offers a high power figures of merit of 1.309 GW/cm² without a penalty on the off-state leakage current.**

***Index Terms*— GaN, AlN, high field effect transistors, HFETs, Breakdown voltage, source field plates, SiNx, power transistors**

I. INTRODUCTION

GaN-based HEMTs have gained significant attention in high-voltage and high-power applications due to the high GaN material breakdown field estimated as ~3.4 MV/cm. But the breakdown voltage scaling with the gate-drain separation does not exceed values of around V_{Br}/d_{GD} = 130 V/µm [1]. A major reason is the non-uniform drift-zone field distribution with particularly high electric field peaks close to the drain-side edge of the gate [3][5]. Source-connected field plates (SFPs) are often used to reduce such field peaks and SFPs overlapping the gate metal (see **Fig. 1a**) are particularly beneficial for fast switching applications since the increased gate-source capacitance helps to stabilize the gate bias against interference from the fast drain-voltage transients [2]. The fabrication of overlapping SFPs requires a dielectric encapsulation layer between the gate metal and the SFP metal. This is usually achieved using a SiN_x layer, which generally gives good passivation properties to GaN HFETs. Depending on the deposition parameters and precursor, PECVD-deposited SiNx layers are often mechanically strained to the AlGaN semiconductor beneath and induce stress to the Schottky-type gate metal. A direct correlation between the increased transistor off-state leakage currents and the SiN encapsulation layer was reported in [4], and a decrease of around 3 orders of magnitude in the leakage current was demonstrated when making an opening in the SiN_x on top of the gate metal. Such strain-release opening, however, would impede the use of overlapping SFPs since the first SiNx layer is interrupted there. In this work we present an approach to still use overlapping SFPs although the 2nd SiN layer was interrupted on top of the gate metal stripes. The void on top of the gate metal was filled with the organic dielectric Benzocyclobutene (BCB) which is soft enough to induce no stress to the gate metal and it thus induces no additional leakage current. The BCB serves as insulator between gate and the SFP, see Figs. 1a and 1b. The initially low leakage current level before the 2nd SiN_x encapsulation is restored after making an opening in the SiN on top of the gate fingers.

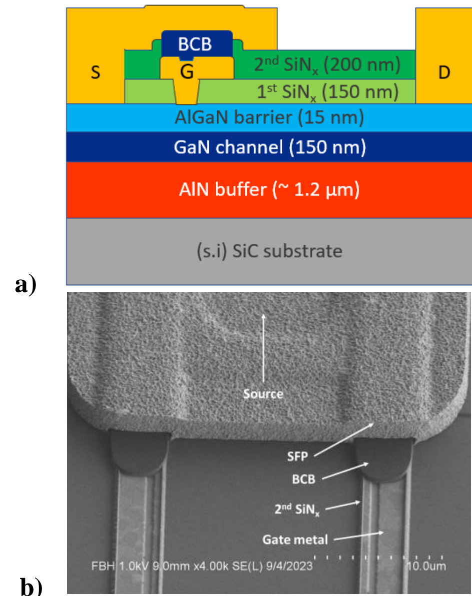

Fig. 1 (a) schematic of the epitaxial structure of the AlN buffer based HFET and **(b)** SEM image of the fabricated devices with SFP

II. DEVICE FABRICATION AND DC MEASURMENTS

The new process module was applied to AlGaN/GaN/AlN HFETs grown by metal-organic vapor-phase epitaxy (MOVPE) on 4" semi insulating SiC substrates (**Fig. 1a**). The AlN buffer layer serves for excellent back-barrier properties which is the root cause for the recently demonstrated excellent breakdown voltage scaling of V_{Br}/d_{GD} = 140 V/µm [3]. An even high breakdown voltage scaling of 150 V/µm was achieved here for an average of 9 transistors of every separation, and transistors with the new SFP technology showed breakdown voltages up to 2370 V for d_{GD} = 15.25 µm. The first 150 nm SiN passivation layer is deposited using plasma enhanced chemical vapor deposition. Ir-based Schottky gates are evaporated on top of a 700 nm long gate trench, which was dry-etched into the 1st SiNx layer. DC characteristics are measured for test devices with source-gate and gate-drain separation (d_{GD}) of 1 µm and 2 µm, respectively. At 10 V drain source voltage, the off-state leakage

current is around 0.97 µA/mm for a gate voltage of -3 V, the maximum current density is 450 mA/, see **Fig. *2***. A 2nd SiN_x encapsulation layer of 200 nm is deposited with the same technique. I-line stepper lithography

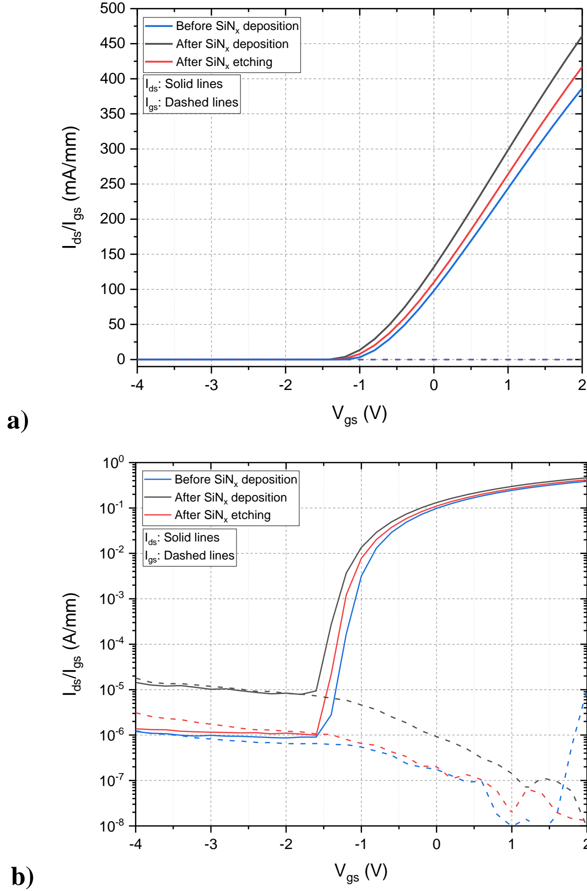

Fig. 2. a) logarithmic **b)** linear scale transfer characteristics of 2x50µm test device measure at 10 V drain voltage before SiN passivation (blue), after SiN passivation (black) and after the SiN opening on top of the gate metal (red). Gate currents are shown in dashed lines and drain currents in solid lines.

defines the etching pattern on top of the gate fingers. The 2nd SiN_x is then etched with SF_6-based reactive ion etching, Spin-coated BCB is used to fill the openings in the SiN_x. Since the minimum thickness that could spin coated is around 1µm, the BCB is etched back and leveled to a thickness of around 300400 nm. This reduces the high morphology and allows for a smooth vertical SFP profile. The BCB outside the gate fingers is then anisotropically etched using a mixture of CF_4 and O_2 in a reactive ion etching process. Then, the Au based SFP metal was then deposited on top by means of electro-plating (Fig. 1b).
The DC measurements in **Fig. 2b** show an increased off-state gate and drain leakage current by around one order of magnitude after the deposition of the 2nd SiNx layer, which we attribute to the layer's tensile stress. The stress level was measured separately on a 4" Si dummy wafer and was determined as 200 MPa. Making an opening in the SiN layer on top of the gate metal resulted in a decrease in the gate leakage current down to 1.67 µA/mm which is close to the initial leakage level before the 2nd SiN deposition. **Fig. *2*b** demonstrates the impact of the tensile strain of the 2nd SiNx layer on the on-state current density. I_D increases from 390 mA/mm to 461 mA/mm after depositing the 2nd SiN layer. When etching the 2nd SiNx on top of the gate metal, some of its tensile strain is released and I_D drops by 60 mA/mm.

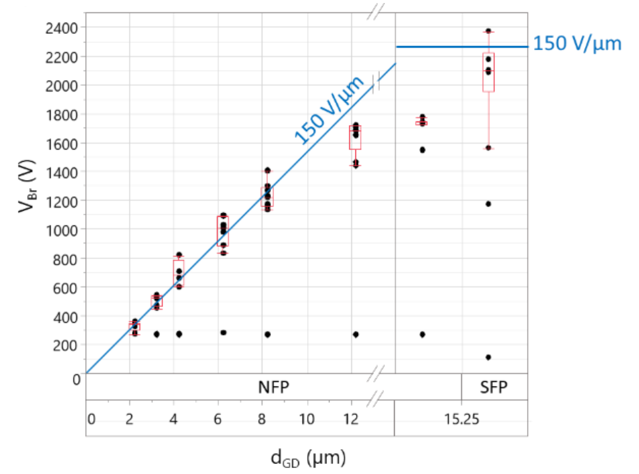

Fig. 3 Breakdown voltage scaling of test devices with gate-drain separation between 2 µm and 15.25 µm w/o FP (NFP) and SFP devices with d_{GD} = 15.25 µm. The wafer distribution of ~9 devices each is displayed.

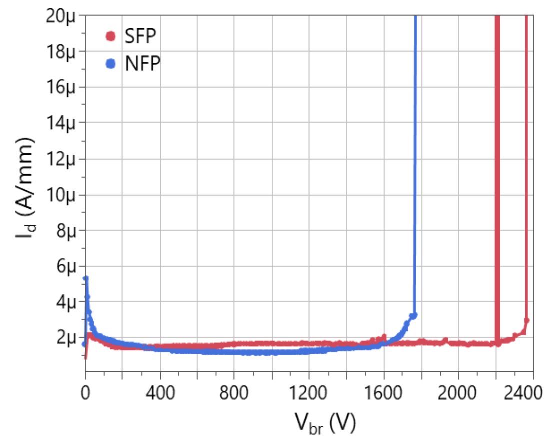

Fig. 4. Breakdown of test devices with gate-drain separation of 15.25 µm without field plates in blue and with SFP in red of the highest performing devices.

The breakdown voltage scaling with d_{GD} for test devices with 0.25 mm gate width is shown in **Fig. 3**. The values were obtained for a hard breakdown at a current level of 1 mA/mm. A slope of 150 V/µm was observed up to 1400 V for d_{GD} = 8 µm without field plates (NFP). However, the breakdown voltage tends to saturate around 1600 V, even for larger d_{GD}. The high observed V_{Br}-scaling could be extended up to d_{GD} = 15 µm when implementing the new overlapping SFP. **Fig. *4*** demonstrate the off-state drain currents for devices with and w/o SFP. A median breakdown voltage of 1732 V was obtained for devices w/o SFPs, while 2100 V was achieved for devices with SFPs (**Fig. 3**), with the highest individual device on the wafer giving 2370 V. Considering the $R_{ON}\cdot A = 4.25\times10^{-3}\ \Omega\cdot cm^2$ of this SFP device a power figure-of-merit of 1.309 GW/cm^2 is obtained, which is among the highest values for GaN-HFET transistors (**Fig. *5***).

III. Conclusion

We report a process module for GaN power transistors using field plates to reach higher breakdown voltages without a penalty on the off-state leakage current induced from the encapsulation layer. The leakage current was found to decrease by one order of magnitude when making an opening the SiN_x passivation layer on top of the gate metal. Filling this opening with BCB made allows the use of overlapping field plates

without sacrificing low off-state leakage current levels. Devices with 15.25 μm gate-drain separation showed a maximum breakdown voltage of 2370 V as compared to 1792 V without a field plate.

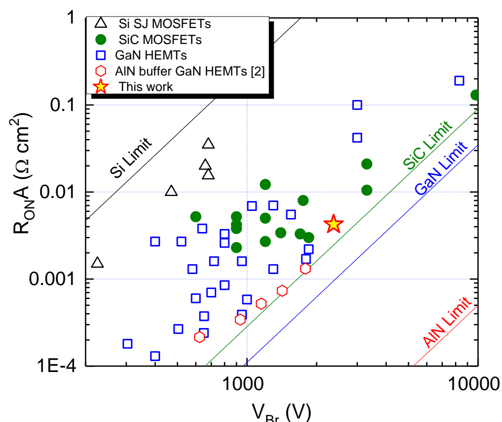

Fig. 5. $R_{ON}\cdot A$ vs. V_{Br} benchmarking of the SFP device of Fig. 4 (star) compared to other technologi

REFERENCES

[1]. Hilt, O., Bahat Treidel, E., Wolf, M., Kuring, C., Tetzner, K., Yazdani, H., Wentzel, A. and Würfl, J. (2019), Lateral and vertical power transistors in GaN and Ga_2O_3. IET Power Electronics, 12: 3919-3927. doi.org/10.1049/iet-pel.2019.0059

[2]. Hilt, O., et al. "10 A/950 V switching of GaN-channel HFETs with non-doped AlN buffer." *2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. IEEE, 2023.

[3]. V. Palankovski, S. Vitanov and R. Quay, "Field-Plate Optimization of AlGaN/GaN HEMTs," 2006 IEEE Compound Semiconductor Integrated Circuit Symposium, San Antonio, TX, USA, 2006, pp. 107-110, doi: 10.1109/CSICS.2006.319926

[4]. Chevtchenko, S. A., et al. "Investigation and reduction of leakage current associated with gate encapsulation by SiNx in AlGaN/GaN HFETs." *2011 International Conference on Compound Semiconductor Manufacturing Technology, CS MANTECH 2011*. 2011.

[5]. Xing, H., et al. "High breakdown voltage AlGaN-GaN HEMTs achieved by multiple field plates." *IEEE Electron Device Letters* 25.4 (2004): 161-163.