5-level stacked $In_{0.53}Ga_{0.47}As$ Multi-Bridged Channel Field-Effect Transistors

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Abstract

We present highly scalable 5-level stacked gate-all-around (GAA) $In_{0.53}Ga_{0.47}As$ multi-bridged channel FETs (MBCFETs) with superior device performance. At the heart of integration process, we maintained temperature of all the unit process under 300 ℃ and inserted an *n*-InP ledge into a top $In_{0.52}Al_{0.48}As$ sacrificial layer to prevent fluorine migration phenomenon. Moreover, a selectively regrown *n*+$In_{0.53}Ga_{0.47}As$ was used in the source/drain regions via MOCVD, together with a precision dry etching at 200 ℃. Particularly, the dry etching process resulted in a highly vertical etching slope along both the S/D and W_g directions. The fabricated L_g = 60 nm MBCFET exhibited excellent DC figures-of-merit (FOMs) with a combination of R_{ON} = 35 Ω·μm, S = 75 mV/decade, g_{m_max} = 19.4 mS/μm & I_{on} = 2.81 mA/μm at both V_{DS} and V_{GS} = 0.5 V, yielding Q (g_{m_max}/S) = 258 mS·dec./V·μm.

INTRODUCTION

The MOSFETs have been innovated to not only maximize device scalability for improving the performance, but also improve gate controllability for ensuring the electrostatic integrity of the device. To simultaneously meet these requirements, the transistor architecture has been evolved from the planar structure to the 3D configuration with high aspect ratio together with gate-all-around (GAA) scheme. Indeed, non-planar and multi-gate architectures have been the backbone of the improved electrostatics in Si MOSFETs. Recently, 3D MOSFETs with sub-10 nm physical dimensions have been reported in numerous channel materials, including Si, Ge and III-Vs. Multi-bridged channel FETs (MBCFETs), also known as the ribbon-FETs, are believed to be the final evolutionally steps for the Moore's law, by providing the best gate controllability and improving the effective channel width by vertically stacking multi-level channel layers [1-3]. As a result, a high-mobility channel material combined with an MBCFET geometry is of great importance since it gives maximization on I_{ON} together with excellent integrity. In this regard, $In_xGa_{1-x}As$ is a promising channel material due to its superior carrier transport properties including very high injection velocity (v_{inj}).

In this work, we present each unit process step in order to fully benefit from the excellent carrier transport properties of the $In_{0.53}Ga_{0.47}As$ nanosheet in the aspect of: i) suppression of F^--migration with a combination of low-temperature integration route and the use of the *n*-InP ledge and ii) a precise and highly controllable dry etching process that enables the fabrication of multi-level stacked MBCFETs with sub-100 nm gate lengths.

FABRICATION PROCESS

Figure 1 highlights an overall integration flow and 3D schematic of an $In_{0.53}Ga_{0.47}As$ MBCFET in this work. The epitaxial layer structure consists of $In_{0.53}Ga_{0.47}As$ multi-quantum-wells (MQWs), sandwiched by each $In_{0.52}Al_{0.48}As$ sacrificial layer. Here, we added an *n*-InP ledge into the top $In_{0.52}Al_{0.48}As$ sacrificial layer to prevent the F^--migration during the device fabrication [4]. **Figure 2 (a)** highlights several key unit process steps. What is different from our previous report [5] is that we developed precision dry etch with a BCl3/SiCl4-based ICP at 200 °C (**step-i**) that enabled a highly vertical etching slope, followed by selective *n*+ $In_{0.53}Ga_{0.47}As$ regrowth by MOCVD and S/D contact formation steps (**step-ii**). Line/space patterns were defined using a positive PR, where the opened regions were etched

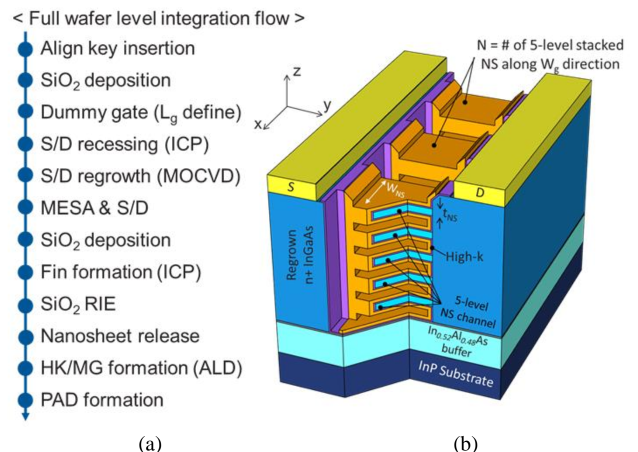


Figure 1. (a) Process flow, and **(b)** 3D schematic of a 5-level stacked GAA $In_{0.53}Ga_{0.47}As$ MBCFET

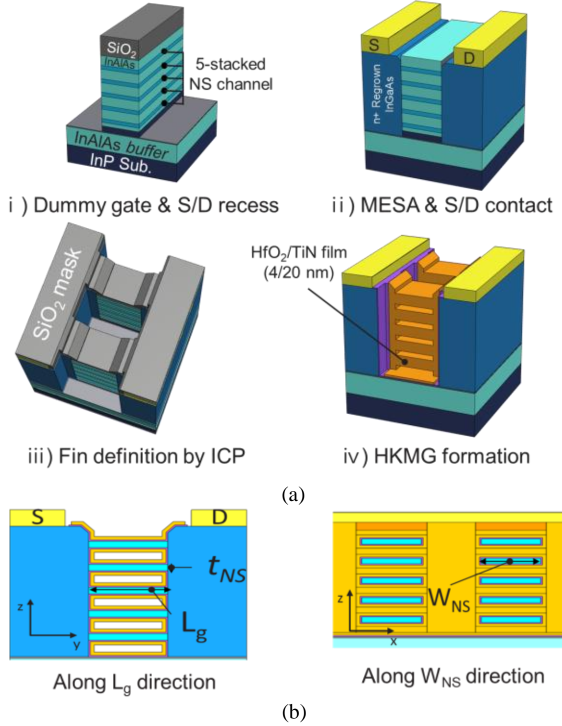


Figure 2. (a) Highlight of key unit process steps of the 5-level stacked **(b)** $In_{0.53}Ga_{0.47}As$ GAA MBCFET and geometrical definitions in this work

vertically through the same BCl3/SiCl4-based ICP at 200 °C, and the $In_{0.52}Al_{0.48}As$ sacrificial layers were etched isotropically with a HCl based solution (**step-iii**). The device fabrication was done with deposition of a 4-nm-thick HfO_x and a 20-nm-thick TiN by ALD (**step-iv**). The ICP-etching process at 200 °C used in this work provided us with the end-point-detection function, where the ICP etching was stopped after the 6th peak of Al-based byproduct was detected. This precision dry etching process yielded a highly vertical etching

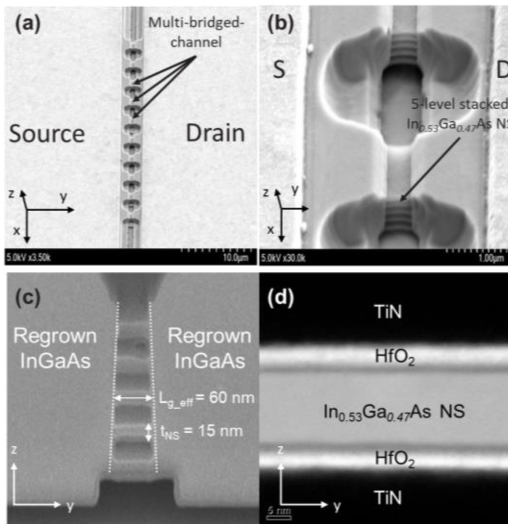
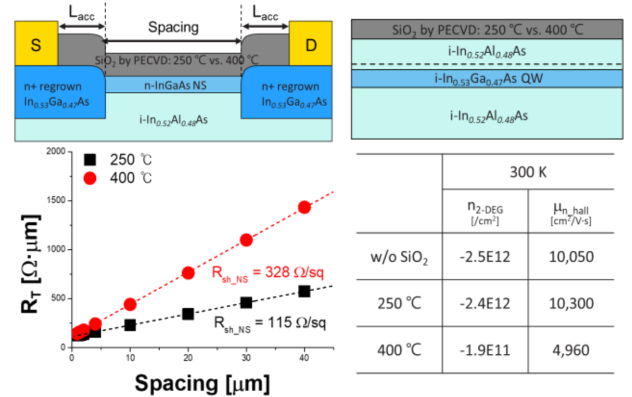


Figure 3. SEM & TEM images of the GAA MBCFET with 5-level stacked $In_{0.53}Ga_{0.47}As$ nanosheets

slope and very clean surface morphology on the etched region that helped to not only improve the geometrical scalability, but also initiate uniform nucleation of the regrown $n+In_{0.53}Ga_{0.47}As$ layer by MOCVD. **Figure 2 (b)** explains the geometrical definition in the proposed MBCFETs, such as W_{NS} (width of a unit nanosheet), t_{NS} (thickness of a unit nanosheet), L_g (gate length) and N (total number of the 5-level stacked nanosheets along the W_g direction), respectively. **Figure 3** shows the tilted and cross-sectional SEM/TEM images for the fabricated MBCFETs in this work.

RESULTS AND DISCUSSION

To evaluate the effect of the F^--migration phenomenon, we fabricated two types of test devices. One are nanosheet TLM patterns and the other are VdP Hall patterns, illustrated in **Figure 4**. Here, SiO_2 was deposited by PECVD at 250 °C and 400 °C, respectively. In our previous report [5], SiO_2 layers were deposited at 400 °C. Both TLM and VDP patterns with SiO_2 deposited at 400 °C condition, showed increased sheet resistance of the NS channel layer, and decreased both $n_{2\text{-}DEG}$ and electron mobility. This indicates that the devices suffered from severe F^--migration phenomenon, whereas the ones with 250 °C were free from those issues. As a result, we maintained the temperature of all the unit process steps below 300 °C, except for the selective regrowth by MOCVD.



	300 K	
	$n_{2\text{-}DEG}$ [/cm²]	μ_{n_hall} [cm²/V·s]
w/o SiO_2	-2.5E12	10,050
250 °C	-2.4E12	10,300
400 °C	-1.9E11	4,960

Figure 4. Evaluation of F^--migration phenomenon using two test structures (NS-TLM and VdP): 250 ℃ vs. 400 ℃.

To evaluate the electrical contact characteristics between the regrown $n+$ $In_{0.53}Ga_{0.47}As$ layer and the 2D $In_{0.53}Ga_{0.47}As$ nanosheet, two types of TLMs were fabricated, as shown in **Figure 5.** One was a regrown TLM to evaluate the contact characteristics between a non-alloyed S/D metal and regrown $n+$ $In_{0.53}Ga_{0.47}As$ region, and the other was a NS TLM to evaluate the resistance between the heavily doped $In_{0.53}Ga_{0.47}As$ layer and the $In_{0.53}Ga_{0.47}As$ nanosheet along the (011) direction ($R_{c\text{-}NS}$). The NS TLM patterns were fabricated and characterized with two different conditions of $n_{2\text{-}DEG}$, such as 2×10^{12} cm^{-2} and 1×10^{13} cm^{-2}. As in [8], $R_{c\text{-}NS}$ can be theoretically given by $R_{c-NS} \cong h/\sqrt{2q^2 n_{2-DEG}}$. The extracted values of $R_{c\text{-}NS}$ at 300 K were 48 and 24 Ω·μm for $n_{2\text{-}DEG}$ =

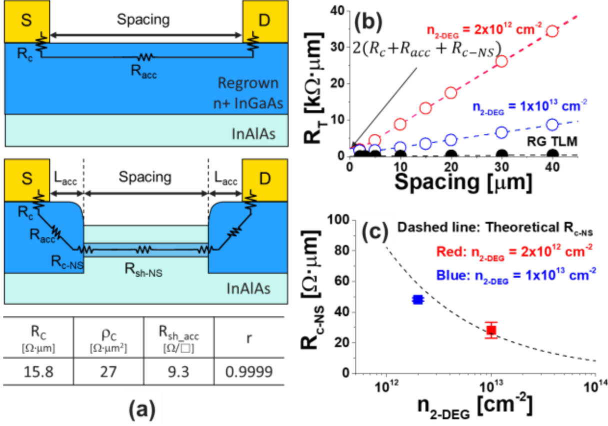
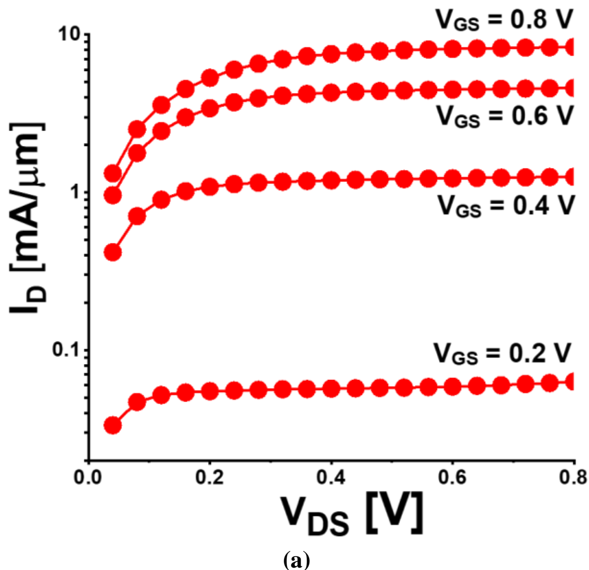


Figure 5. Measured results on a TLM for the regrown $In_{0.53}Ga_{0.47}As$ and a NS-TLM, together with theoretical projection.

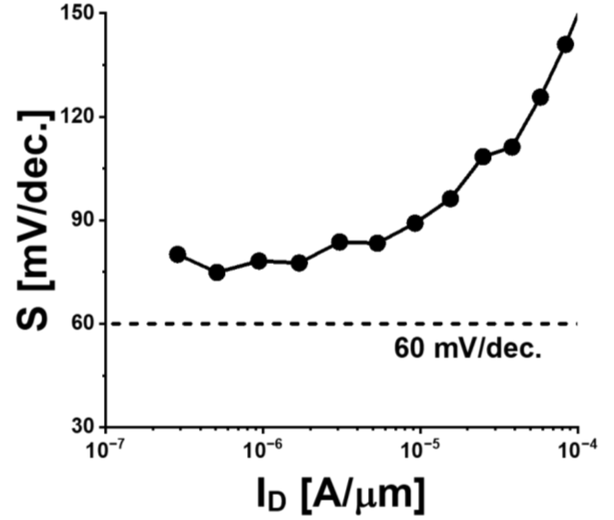
2×10[12] and 1×10[13] cm[-2], which are close to the theoretical calculation from the equation above.

Figure 6 (a) shows the DC characteristics of a fabricated L_g = 60 nm $In_{0.53}Ga_{0.47}As$ MBCFET in this work. Here, the device characteristics were normalized by the footprint of each nanosheet channel layer. From the output characteristics, the device exhibits a very small value of R_{ON} = 35 Ω·µm at V_{GS} = 0.8 V and excellent drain current saturation characteristics up to V_{DS} = 0.8 V, providing I_{ON} = 2.81 mA/µm at V_{GS} = V_{DS} = 0.5 V. **Figure 6 (b)** plots the measured subthreshold swing (S) and transconductance (g_m) characteristics as a function of I_D at V_{DS} = 0.5 V, for the same device. The device exhibited a minimum value of subthreshold swing (S) = 75 mV/decade and $DIBL$ = 10 mV/V. g_m has excessed of 3 mS/µm even with V_{DS} = 0.05 V, and the peak g_m was as high as 19.4 mS/µm with V_{DS} = 0.5 V, indicating that each $In_{0.53}Ga_{0.47}As$ NS channel layer exhibits 3.8 mS/µm equivalently.

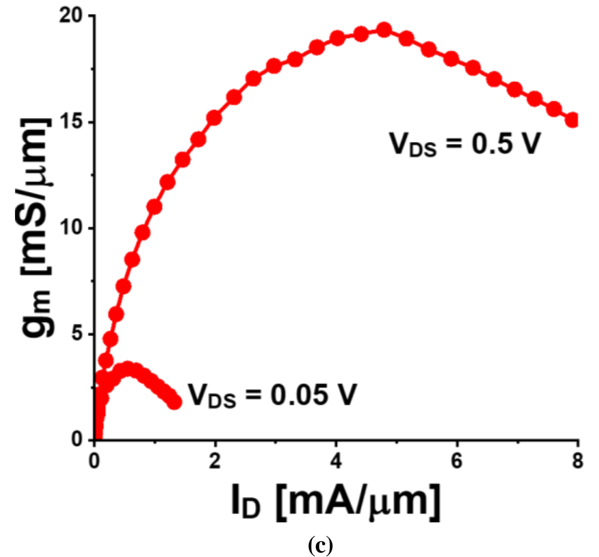
Finally, Q was defined as g_{m_max}/S, which integrates carrier transport property and electrostatic integrity. The fabricated L_g = 60 nm 5-level stacked $In_{0.53}Ga_{0.47}As$ GAA MBCFET in



(a)



(b)



(c)

Figure 6. DC characteristics of the fabricated L_g = 60 nm MBCFET in this work: **(a)** output characteristics, **(b)** the measured subthreshold swing (S), and **(c)** g_m characteristics as a function of I_D at V_{DS} = 0.05 V and V_{DS} = 0.5 V.

this work exhibits the highest g_{m_max} in any FET technologies. Moreover, the device in this work represents the best balance between g_{m_max} and S, yielding a value of Q = 258, which is the highest value ever reported.

Conclusions

In this work, we successfully demonstrated a scalable $In_{0.53}Ga_{0.47}As$ GAA MBCFET technology with 5-level stacked $In_{0.53}Ga_{0.47}As$ nanosheet channel layers. Mitigation of fluorine migration and highly controllable dry etching process enabled the fabrication of a L_g = 60 nm MBCFET with excellent logic FOMs of S = 76 mV/decade, $DIBL$ = 10 mV/V, I_{ON} = 2.81 mA/µm, g_{m_max} = 19.4 mS/µm and Q = 258 at V_{DS} = 0.5 V. These device figures-of-merit represent the best

balance of S, g_{m_max} and Q among all the non-planar MOSFET technologies ever reported.

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ACRONYMS

MBCFETs: Multi-bridged channel Field Effect Transistors
NS: Nanosheet
GAA: Gate-all-around