Wafer Bow Tuning with Stealth Laser Patterning for Vertical High Voltage Devices with Thick GaN Epitaxy on Sapphire Substrates

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Abstract

In this work we present a systematic study on a novel method to reduce the very strong bow of 4-inch GaN-on-sapphire wafers with more than 15 µm thick epitaxy. Laser scribing of the epitaxial grown sapphire substrates results in monotonically increase of the wafers radius of curvature and a bow reduction from 300 µm to 50 µm with respect to the scribing pitch. Quasi-vertical *pn*-diodes are used to electrically-monitor changes to the epitaxial layers as a result of the substrate laser scribing process. The quasi-vertical *pn*-diodes manufactured in industrial process line on bow-reduced wafers have demonstrated median reverse bias blocking strength of ~1150 V and specific on-state resistance of ~1.5 mΩ·cm². It was identified that the reverse bias current is mostly dominated by the pre-existing epitaxial defects and that the substrate laser scribing did not hinder the epitaxy performances.

INTRODUCTION

Vertical GaN-based power switching devices, diodes and transistors, are particularly desirable due to their reduced die size in comparison to lateral heterostructures based devices. This results in a reduction of specific ON-state resistance, $R_{DS\_ON} \times A$, by one order of magnitude down to 1.0 mΩ·cm² [1-2]. The targeted blocking capability larger than 1.2 kV demands the growth of n^--GaN drift layers thicker than 10 µm [6] with low residual background doping. However, the drift region conductivity may be limited by background compensating doping, high defect density, built-in potential barriers and low mobility, having a direct impact on the device electrical performance. Vertical GaN power switching devices with low specific ON-state resistance require highly conductive GaN substrate, ~10^{-3} Ω·cm. These substrates allow homoepitaxial growth of very thick GaN drift layers with very low internal strain that result in low wafer flatness distortion / bow. In contrast, GaN substrates are limited in their size < 100 mm and conductivity. Furthermore, GaN substrates are very expensive, ~ 150 USD/cm², and limited in their availability. Therefore, it is suggested manufacture these devices on foreign substrates, Si or sapphire. [3]

The backside drain contact may be then established after local Si substrate removal [4] or laser liftoff sapphire substrate removal [5]. Previously, we provided an optimization procedure for designing the drift layer properties for a given voltage rating [6]. However, growing thick GaN epi-layers > 10 µm is especially challenging on foreign substrates where the interface lattice mismatch and thermal coefficient differences generate a series of undesirable effects, such as increase of threading dislocations density, increased leakage current, increased mechanical strain and fragility and increase in wafer bow. In this work we will report the issues of growing thick (> 5 µm) GaN drift layer on sapphire substrates for vertical high voltage GaN devices and how to cope with the resulting high wafer bow that would make these wafers un-processable on commercial equipment designed for flat silicon wafers.

Cho *et al.* [7] reported a way to reduce bow in GaN-on-sapphire based UV-LED wafers using a focused laser in order to selectively introduce localized damage inside the sapphire substrate close to the backside surface to compensate the internal stress caused be the epitaxy growth. This method showed to be effective at reducing the overall bow for 2-inch sapphire wafers with less than 450-µm overall thickness, however, in order to be usable in larger scale processing, this method needs to be proven for larger wafers with even thicker GaN epitaxial layers as well. 4-inch GaN-on-sapphire wafers with a total GaN-layer thickness larger than 15 µm are studied in this work.

TABLE I WAFER BOW AND LASER STEALTH SCRIBING DATA SUMMARY

Wafer	Pitch$_{(x, y)}$ (µm)	Before patterning		After patterning	
		R_x (m)	R_y (m)	R_x (m)	R_y (m)
"A"	35	3.71	3.65	6.58	6.72
"B"	30	3.79	3.62	7.18	7.18
"C"	25	3.79	3.76	8.11	7.96
"D"	20	3.73	3.88	7.81	7.96
"E"	15	3.69	3.54	11.26	11.57
"F"	10	3.69	3.54	20.16	26.02
"G"	10	3.73	3.88	21.55	31.72

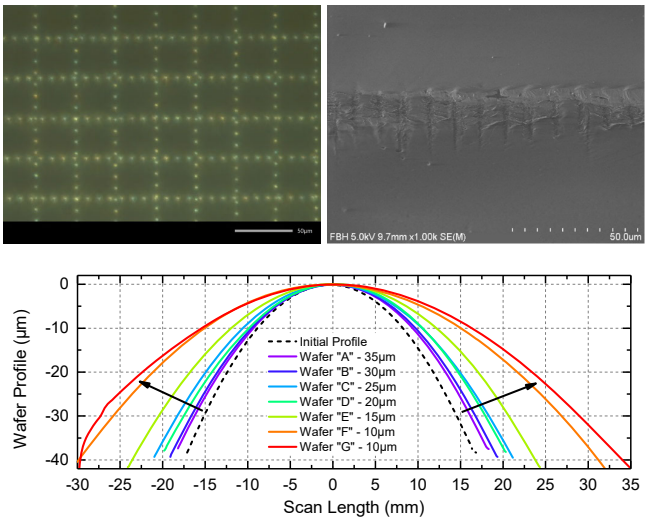
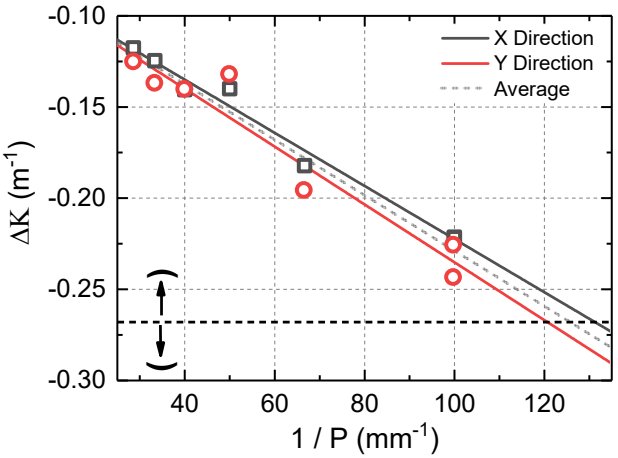


Fig. 1. (left) Laser grid pattern top view with 30 µm pitch. (right) Cross-section of the laser damage along one scribe line with 40 kHz laser frequency and 400 mm / s scribing speed, resulting in 10 µm of laser spacial period. (bottom) optical interferometric wafers' bow profile for the different scribing pitch.

After epitaxy, these wafers feature a typical initial bow of ~300 µm, which corresponds to a wafer curvature radius of ~3.8 m. Industrial process lines, such as in Ferdinand-Braun-Institut, may tolerate wafer bow below smaller than 125 µm which correspond to a wafer curvature radius of larger than 10 m. However, wafers with high bow within process limitations may still present conformity issues, due to wafer vacuum handling, un-even temperature exposure, coating thickness etc. In this work we will show the results of different laser-scribed GaN-on-sapphire wafers by using both, bow measurements and electrical measurements for processed quasi-vertical *pn*-diodes, in order to assess both the effectiveness of the technique as well as the impact on the final electronic device performances.

EXPERIMENTAL SETUP

The experiment starts with identical 650 µm thick 4-inch sapphire substrates. Double side polished substrates are chosen for easiness of optical monitoring of the laser induced damage. The MOCVD-grown GaN epitaxial layer stack consists of a 2.2 µm un-intentionally doped GaN buffer layer, a 2.4 µm n^+-GaN:Si (N_D = 3.0 × 10^{18} cm^{-3}) highly conductive cathode bottom layer and a 10 µm n^--GaN:Si drift layer with N_D = 1.4 × 10^{16} cm^{-3}. The drift layer doping concentration is monitored by electrochemical capacitance voltage (ECV) measurements and post-processing CV measurements. A 500 nm *p*-GaN:Mg 1 × 10^{19} cm^{-3} layer and an additional 30 nm *p*-GaN:Mg 2 × 10^{19} cm^{-3} anode contact-layer are regrown and in-situ activated in a separate MOVPE reactor. The approximate initial wafer bow after epitaxy is ~300 µm



$$\Delta K_x = \frac{1}{R_x} - \frac{1}{R_{x_0}} = -\frac{1.46}{P[\mu m]} - \frac{1}{13.03}$$

$$\Delta K_y = \frac{1}{R_y} - \frac{1}{R_{y_0}} = -\frac{1.59}{P[\mu m]} - \frac{1}{13.06}$$

$$\overline{\Delta K} = \frac{1}{R} - \frac{1}{R_0} = -\frac{1.52}{P[\mu m]} - \frac{1}{13.05}$$

Fig. 2. (top) $\Delta K = (\frac{1}{R} - \frac{1}{R_0})$ vs reciprocal laser pitch fitted with Eq. 1 and extracted parameters for *x* (1st scribe) and *y* (2nd scribe) direction. (bottom) *x*, *y* and average fitting parameter using Eq. 1.

(R ~3.8 m) for all wafers. Laser patterning is carried out after epitaxy, with different laser pitches and fixed focus depth resulting in a damage being located at 200 µm above the bottom surface of the sapphire substrate. The patterning was realized by focusing a laser beam in the sapphire close to its back surface, irradiated from the top side through the epitaxy layers, using a laser scriber (WSS4000) from Opto System Co. Ltd., which uses a Talisker Ultra Laser from Coherent. This means that the laser will be focused inside the sapphire material and, at this position, the crystal will be modified. The used wavelength is 532 nm. Used, the repetition rate is 40 kHz at a feed speed of 400 mm/s and the continuous laser power is 160 mW. The processing procedure starts with the wafers being mounted on a film frame (Disco-type 6") with a UV-tape from Lintec (Adwill D-210), then, the laser is aligned following the wafers´ flat and the scribing pattern lines run perpendicular to the flat with the wanted pitch. This is done in both *x*-direction (1st scribe perpendicular to the flat) and *y*-direction after. The tape is then cured with UV light and the wafer is demounted. Total processing time is ~4 h/wafer. The resulting wafer top view and cross-sectional views of the grid patterns created inside the sapphire substrate are shown in Figs. 1 (left) and (right), respectively.

Resulting wafer bow pre- and post-patterning with different scribing pitch are reported in Table I. Figs. 1 (bottom) depicts the wafers' optical interferometric bow profile for the

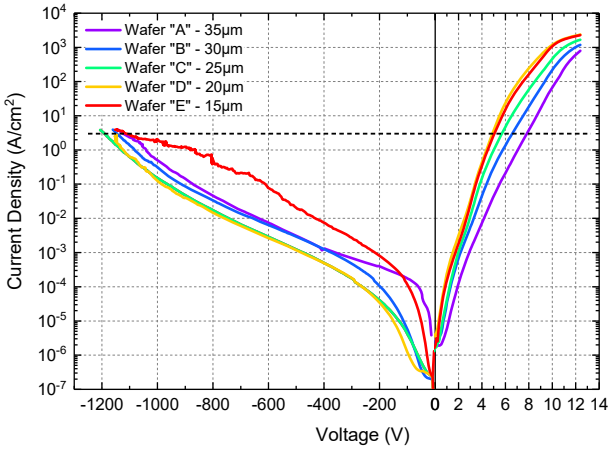


Fig. 3. Wafer-level median revers and forward characteristics of quasi-vertical *pn*-diodes manufactured on wafers "A"-"E"

different scribe density. It is shown that the wafer bow is progressively reducing with the decrease of the pitch and a minimum bow of 41 µm was obtained for wafer "G".
This follows the expected behavior reported by Cho *et al.* and the curvature radiuses follow the same relation, although with parameters A and B to be adapted:

$$\frac{1}{R} - \frac{1}{R_0} = -\frac{A}{P} - \frac{1}{B} \quad (1)$$

Where R_0 and R are the wafer curvature radius before and after patterning, P is the laser patterning pitch and A and B are fitting parameter that are unique for this specific substrate material, thickness and size. Fig. 2 depicts the resulting change in wafers curvature as a function of the laser patterning pitch and the calculated fitting parameters. To demonstrate the processability and the effectiveness of the technique for bow-reduced wafers, we successfully processed quasi-vertical *pn*-diodes using i-line stepper lithography as reported in [6, 9]. Electronic devices, such as these diodes, are very sensitive monitoring tool to detect changes and degradation in the GaN material caused by damaging the sapphire substrate. For this comparison wafers "A"-"E" with bow values reported in Table I after laser patterning are used for the quasi-vertical *pn*-diodes manufacturing, wafers "F"-"G" are only used in this paper as correlation data of the bow reduction process to confirm the proposed model and do not have electrical devices on them.

RESULTS AND DISCUSSION

The processed circular *pn*-diodes with an anode diameter of 200 µm are characterized in DC forward conductance and reverse blocking regime. The wafer level median diode characteristics are summarized in Fig. 3. The wafer level breakdown values and the OFF-state reverse bias leakage at -650 V are summarized in Fig. 4. It is observed that the average ON-state resistance for all diodes is within

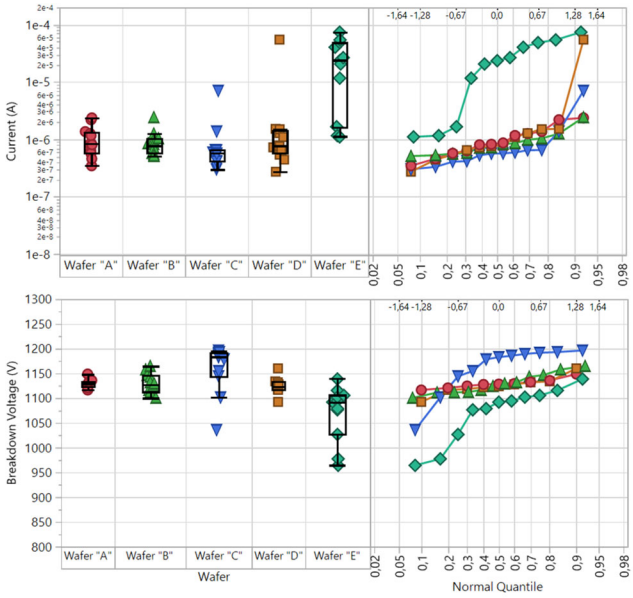


Fig. 4. Wafer-level statistics of (top) reverse biased leakage currents at V = -650V and (bottom) breakdown voltage for *pn*-diodes on wafers "A" to "E"

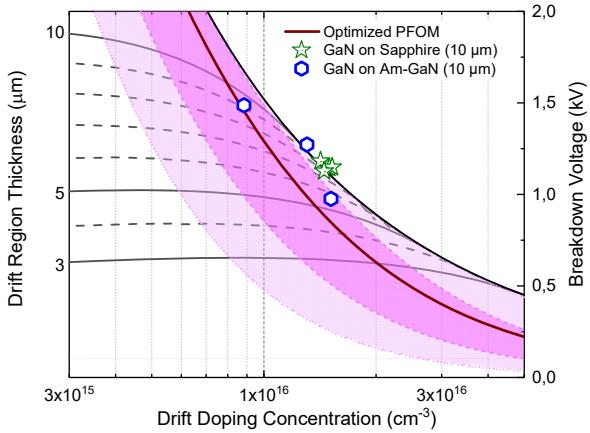


Fig. 5. GaN on sapphire performances comparison with the ideal breakdown voltage values, PFOM values from [3, 8].

expectations of ~1.5 mΩ·cm^2, but the diodes onset voltage is lowered by around ~3 V with the reduction of the scribing pitch. Less pronounced correlation to the laser-scribing pitch is observed for the reverse bias current. The *pn*-diodes on all wafers show reverse current of ~10^{-6} A at -650 V and median breakdown at ~ -1150 V, defined at leakage current level of 3 A/cm^2, independently from the laser pitch. As exception, diodes on wafer "E", with scribing pitch of 15 µm, show higher revers leakage of ~3×10^{-5} A at -650 V but the resulting median breakdown is still ~ -1100 V. Fig. 5 shows the *pn*-diodes breakdown voltage as a function of the drift region ECV-assessed doping concentration. The devices

breakdown, limited by high reverse leakage current, is close to the parallel plane theoretical limit [6]. The breakdown characteristics of the different diodes did not show avalanche behavior, rather it is limited by high reverse leakage current, as similar leakage was observed in *pn*-diodes on non-scribed wafers with similar drift region doping concentration [9]. Therefore, for 1.2 kV rated vertical power devices, farther reduction of the effective doping concentration and improvement of the GaN-on-sapphire epitaxial layers growth are required.

The *pn*-diodes reverse leakage low dependence of the sapphire substrate scribing pitch for the wafer bow reduction indicates that it is originated from pre-existing epitaxial layers defects and it´s not further compromised by the laser damage for laser pitch down to 20 µm, with some effects visible for wafer "E". Likewise, the forward specific ON-state resistance is unchanged. On the other hand, the positive shift in the *pn*-diodes onset voltage may indicate change in the epitaxial layers strain that results in added piezo-electric charge in the *pn*-junction or the *p*-type ohmic contact.

CONCLUSIONS

In this work, we have shown a controlled method to reduce the large bow on 4-inch GaN-on-sapphire wafers with very thick epitaxial structure. The sapphire substrate laser patterning of the epitaxial wafers with different scribing pitch results in monotonic increase of their radius of curvature namely reduction of the wafers' bow. Such 4-inch GaN-on-sapphire wafers with total epitaxial layers thickness larger than 15 µm and initial wafer bow larger than 300 µm were fully processed with quasi-vertical *pn*-diodes in and industrial process line.

It is demonstrated that the manufactured *pn*-diodes reverse bias OFF-state current and blocking strength are minorly influenced by the substrate laser scribing pitch density and may be related to pre-existing epitaxial defects and dislocations. However, the *pn*-diodes onset voltage is strongly dependent on the laser scribing pitch which could indicate changes in the epitaxial layers strain. We can conclude that the sapphire substrate laser scribing for thick GaN epitaxial drift layers can pave the way for large volume manufacturing process towards 1.2 kV vertical GaN devices on low-cost foreign substrates, but it will still require improvement of the epitaxial layers in terms of drift region carrier concentration and reduction of epitaxial originated defects.

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ACRONYMS

USD: United States Dollar (currency)
TLM: Transmission Line Model
UV LED: Ultra Violet Light Emitting Diode
ECV: Electrochemical Capacitance Voltage
MOVPE: Metal Organic Vapor Phase Epitaxy
PFOM: Power Figure of Merit