200-mm Enhancement-mode low-knee-voltage GaN-on-Si MISFETs for high-frequency handset applications

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Abstract

This paper demonstrates a high-performance enhancement-mode GaN-on-Si insulating-gate technology that holds a great potential for the up-coming 6G FR3 frequency band (7GHz to 24GHz) applications. 0.25 um transistors were fabricated with a fully CMOS-compatible process using standard 200 mm Si-fabrication tools. The transistor demonstrated Idmax of >1.1 A/mm, max transconductance >700 mS/mm, Ron < 0.9 ohm-mm, and f_T/f_{max} of 60 GHz/100 GHz. Load pull measurement achieved a >16dB transducer gain and >60% PAE with excellent AM-AM, AM-PM performance at 8 GHz and Vdd of 5 V.

INTRODUCTION

The 6G wireless communication frequency range of 7 GHz to 24 GHz, also known as FR3, has attracted a lot of interest because of its higher data capacity over the existing FR1 (sub-6 GHz) band while avoiding the drawbacks of FR2 (millimeter-wave) band with lower attenuation and longer range. The GaAs HBT technology, which has been the choice for sub6-GHz RF-front-end (RFFE) modules in handsets, struggles to maintain the gain and efficiency as frequencies increase above 6 GHz, while the Si RFSOI technology, currently used for FR2, does not have enough output power needed for FR3. A new semiconductor technology with high performance, high output power and low cost is highly desirable for the 6G FR3 deployment.

Among a few technology candidates, GaN-on-Si technology is very attractive for its low cost and high-power handling capabilities. So far, most GaN-on-Si RF transistors reported are for base-station applications with Vdd of 28 V [1] and are depletion-mode (Dmode) FETs [2], which are not suitable for handset applications. Then et al. [3] are the very few who have demonstrated sub-100 nm deeply-scaled 300 mm GaN enhancement-mode (Emode) FETs for low Vdd operations using InAlN/GaN epi-structure.

In this paper, we demonstrate the first 200 mm Emode GaN-on-Si platform based on an AlGaN/GaN material system for FR3 handset applications. With a gate length of 0.25 um and standard 200 mm Si fab tools, a record device performance in its class can be achieved, demonstrating the potential of this technology platform.

FABRICATION

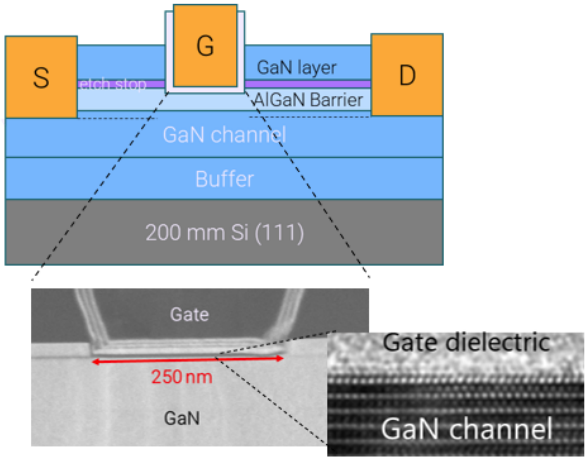

Fig. 1. Transistor structure and TEM showing Lg of 250 nm and gate dielectric interface.

Emode insulating-gate transistors were fabricated with 200 mm GaN-on-Si wafers with an "etch-stop" epi-structure [4], where an AlN etch-stop layer is inserted between a thin AlGaN barrier and a GaN cap layer, as shown in Fig. 1. A low-damage, selective gate recess etch was developed to form an Emode gate trench into the GaN cap-layer. 2-finger RF devices were fabricated with a source-to-drain distance Lsd of 700 nm, gate length Lg of 250 nm and Wg of 50 um per finger. 4 nm ALD Al_2O_3 dielectric was used for the gate insulator. Gate, ohmic and interconnect metals were selected from aluminum, titanium, and titanium nitride. The transistor was passivated by standard PECVD dielectric and has no source field-plate.

N++GaN-regrowth was used to achieve a low ohmic contact resistance Rc of 0.126 ohm-mm. Fig. 2 shows the Rc and Rsh (520 ohm/sq) maps of the wafer. 56 sites across the 200 mm wafer were measured with an edge exclusion of about 10 mm. The Rc and Rsh standard deviations are 0.014 ohm-mm and 16 ohm/sq respectively, which are 11% and 3% of the median values, demonstrating a high within wafer uniformity. Further improvement of Rc and its uniformity can be accomplished by process optimization to achieve 0.1 ohm-mm.

DEVICE CHARACTERIZATION

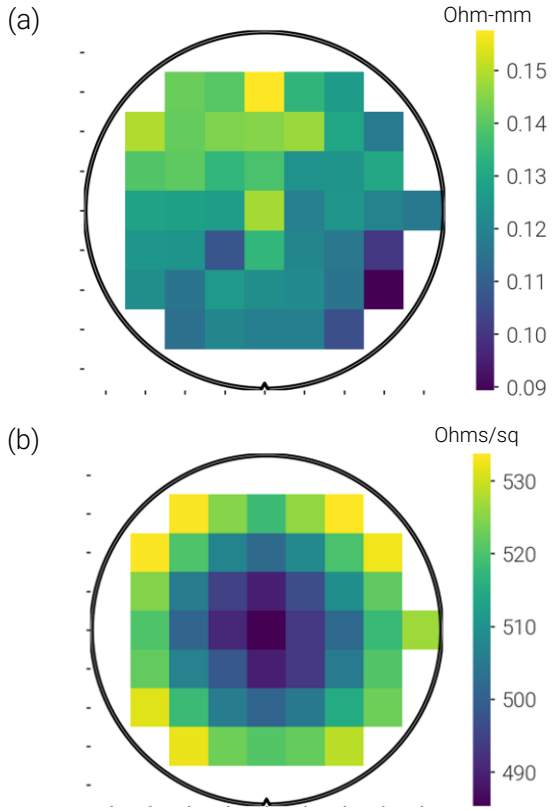

Fig. 2. Mapping of TLM measurements of 200 mm GaN-on-Si wafer: (a) Contact resistance Rc; (b) Sheet resistance Rsh.

As shown in the DC measurement in Fig. 3, the Emode FET has a knee voltage Vknee around 1 V, on-resistance Ron of 0.8-0.9 ohm-mm, peak transconductance g_m up to 760 mS/mm and a threshold voltage Vth around 0.15 V. Pulse IV measurements with 600 ns pulse width at quiescent drain and gate voltages of Vdq = 10 V and Vgq = -0.5 V show minimal trapping with current collapse less than 10% around the Vknee voltage. The device has a subthreshold swing of 80 mV/dec and a negligible DIBL of 40 mV/V, demonstrating a MIS-interface with very low interface state density. Breakdown voltage is measured at Vgs = -1 V, -2 V and -3 V on the same device where a drain-to-source punch-through is observed for Vgs = -1 V and -2 V. Destructive breakdown occurs at Vds = 30 V and Vgs = -3 V caused by gate dielectric reverse breakdown resulting in permanent increase of gate leakage. The off-state leakage of the transistor is typically less than 1 uA/mm, orders of magnitude lower than the conventional Schottky-gate Dmode GaN FETs. Further optimization of the epi with reduced GaN channel background doping and better back barrier are expected to improve the punch-through voltage.

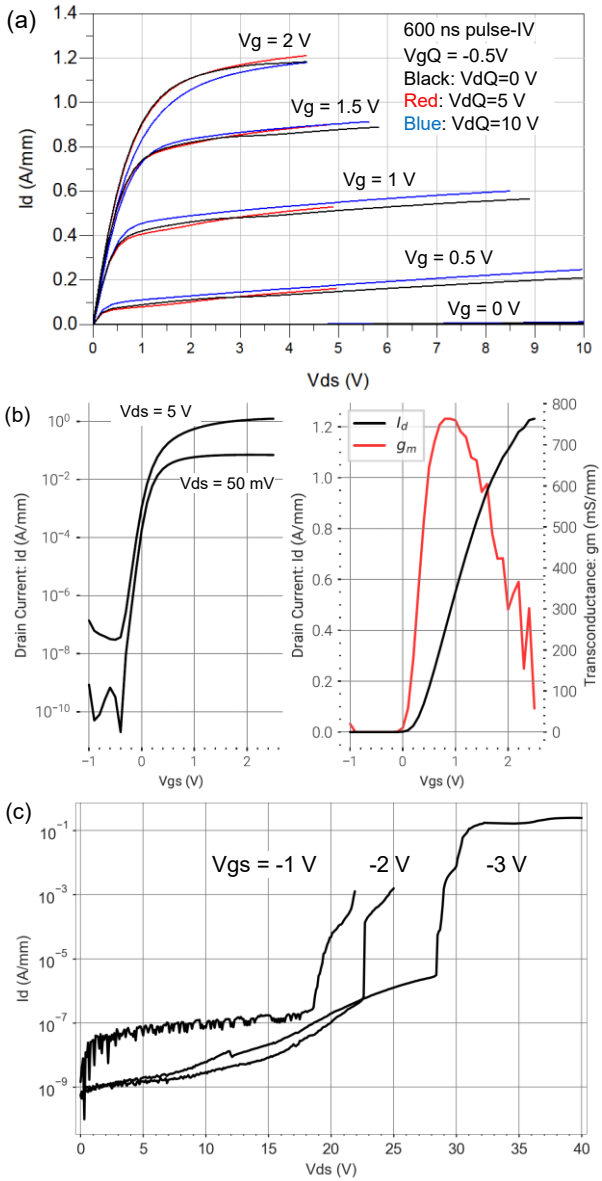

Fig. 3. DC measurement of the 2x50 um Lg = 0.25 um FET. (a) 600ns pulsed IV; (b) Subthreshold Id-Vgs measurement at Vds = 50 mA and 5V; Transconductance measured at Vds = 5 V. (c) Breakdown voltage measurements at different Vgs bias voltages. Destructive breakdown occurs at around 30 V.

Small signal S-parameter measurement results are shown in Fig. 4, where the extracted f_T is typically between 60-65 GHz and fmax between 100 and 110 GHz. The calculated average electron saturation velocity from $Vave = 2\pi f_T \times Lg$ is 0.94-1.0E10^7 cm/s, indicating low parasitic delays [5]. fmax is limited by the relatively high gate resistance of the thin Al gate metal. Improvement in gate resistance can be achieved with standard CMOS back-end process such as Cu-based interconnects.

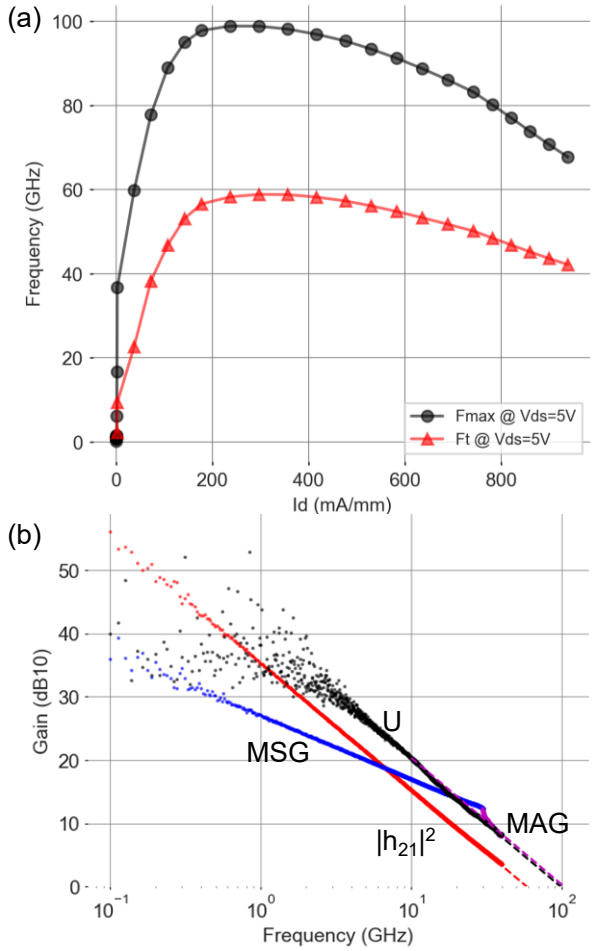

Fig. 4. Small signal measurement of the 2x50 um Lg = 0.25 um FET. (a) ft and fmax as a function of Id; (b) RF gain vs frequency at Id=300 mA/mm and Vds = 5 V.

Large-signal load pull measurements were conducted at 8 GHz, 13 GHz and 26 GHz, shown in Fig. 5. The source and load impedances at the fundamental frequency were tuned for maximum power added efficiency PAE while the impedances at the 2nd and 3rd harmonics were both set to 50 ohms. The FET demonstrated 16 dB and 14 dB transducer gain with PAE of 62% and 56% at 8 GHz and 13 GHz respectively. At 26 GHz, the device gain and PAE are reduced to 9 dB and 45%, due to the limitation of the relatively large Lg and gate resistance. A device with Lg of 220 nm and 2x20 um Wg can improve the gain to 12 dB and 51% PAE at 26 GHz.

To demonstrate the device operation with the condition of envelope tracking, the load pull measurement was performed with Vdd stepping from 1 V to 5 V while the load impedance was kept the same at Vdd = 5 V. Device gain and PAE were above 13 dB and 50% when Vdd was reduced to 2 V, showing good potential for envelope tracking operation. To improve the performance at Vdd = 1V, Ron lower than 0.8ohm-mm can be accomplished with further reduction of Rc and a better matching condition for Vdd = 1 V can also be applied. The device demonstrated good linearity with AM-PM within 1.5 degree for AM-AM compression up to 3.5 dB at Vdd of 2 V to 5 V. The GaN FET is capable of operating at higher Vdd than 5 V. For example, measurements at Vdd = 8 V, showed a gain of 17 dB and PAE of 60% at 8 GHz with a Pout of 21 dBm, reaching over 1.25 W/mm, demonstrating the advantage of GaN over GaAs in its capability of operating at higher Vdd and power density.

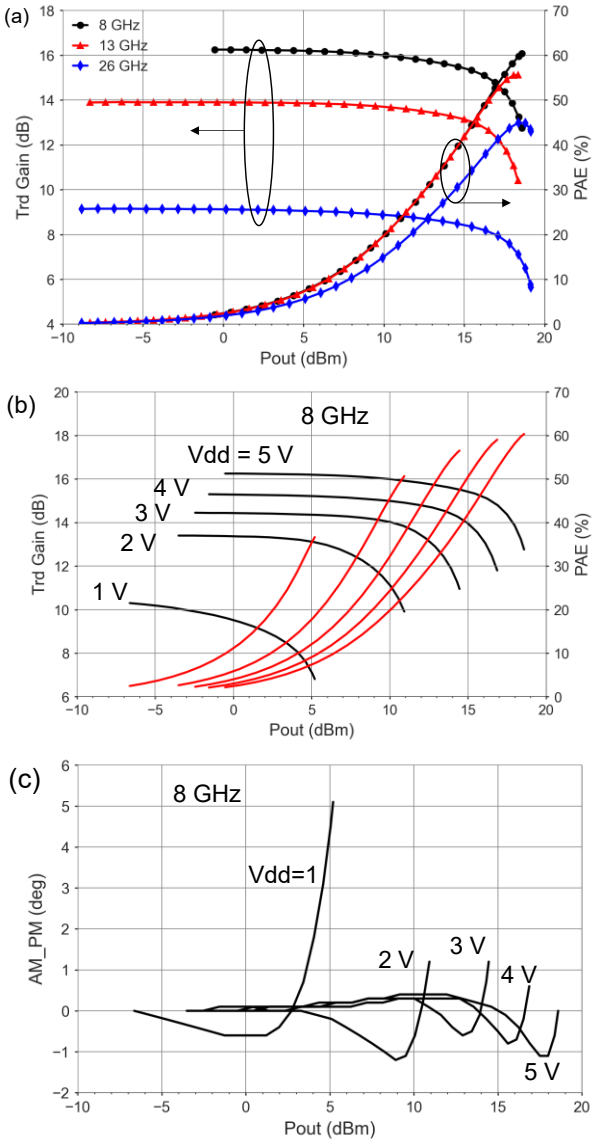

Fig. 5. Large signal measurement of the 2x50 um Lg = 0.25 um FET. (a) Transducer gain and PAE vs Pout at 8, 13, and 26 GHz and Vd = 5 V; (b) Load pull with Vd of 1 V to 5 V at 8 GHz; (c) 8 GHz AM-PM within 1.5 degree for AM-AM within 3.5dB and Vd from 2 to 5 V.

DEVICE MODEL

Physics-based MIT Virtual Source GaNFET (MVSG) compact model [6] illustrates the impact and limitations of the access regions to the transistor performance. Physical dimensions and parameters were used to fit the measured pulse-IV data at Vdq = 0 V and Vgq = -0.5 V without trapping and self-heating effects. The effects of the electron velocity saturation of the 2DEG in the transistor access region is modeled as virtual-gate transistors [7] with a saturation velocity of 1E7 cm/s, as shown in Fig. 6a by the black-solid lines - the "transistor model". The model has a good fit to the measurement. Replacing the "virtual-gate transistors" for the access regions with resistors (blue-dashed-lines in Fig.6a) without velocity saturation effects demonstrates the deviation of the Id-Vd curves from the measured data for Id current density above 0.6 A/mm. Without limitations of the 2DEG velocity saturation in the access regions, the transistor would have reached to a higher Idmax of 1.4A/mm and sharper Vknee of 1V at Id > 1A/mm. The gm would have shown a much flatter shape as shown in Fig. 6b – "resistor model", instead of a steep drop for Vgs above 1 V or Id above 0.6 A/mm.

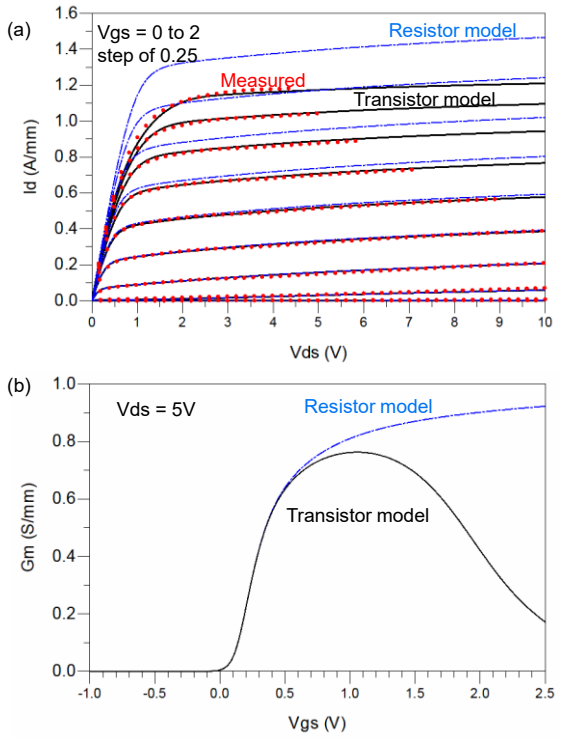

Fig. 6. Comparison of MVSG compact model vs. measurement. (a) Effect of velocity saturation in the access regions of the transistor on knee voltage and Idmax: Black-solid curves are MVSG model using "virtual-gate transistors" for the access regions vs blue-dashed curves using resistors for the access region; (b) Effect of velocity saturation in the access regions of the transistor on the shape of the Gm curve.

CONCLUSIONS

This paper demonstrated the first Emode AlGaN/GaN based 200 mm GaN-on-Si RF FETs with Lg of 0.25 um and a performance with relatively small parasitic impacts such that it reaches 1E7 cm/s average electron velocity. Physics based compact model reveals that the Idmax, Vknee, and drop of gm are limited by the electron velocity saturation in the access regions. With the low-cost of Si-CMOS compatible fabrication, this Emode 200 mm GaN-on-Si technology shows a great potential for FR3 handset applications.

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
PECVD: Plasma Enhanced Chemical Vapor Deposition
ALD: Atomic Layer Deposition
DIBL: Drain Induced Barrier Lowering
2DEG: Two Dimensional Electron Gas