SmartSiC™ 150 & 200mm engineered substrate: increasing SiC power device current density up to 30%

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Abstract

The Smart Cut™ technology enables the integration of high quality SiC layer transfer for device yield optimization, combined with a low resistivity handle wafer (below 5mOhm.cm) to lower device conduction and/or switching losses both for 150mm and 200mm wafers diameter. Based on material characterisation, we anticipate a benefit of up to 15% or 30% in terms of RDSon for state of the art 1200V SiC MOSFET and JFET. 1200V SiC diodes and MOSFETs have been fabricated by Fraunhofer IISB. 1200V diodes (JBS and MPS) with voltage drop improvement by 12% at rated current have been demonstrated. Lowering of the development of SSF is demonstrated after UV illumination opening the path for robustness to bipolar degradation.

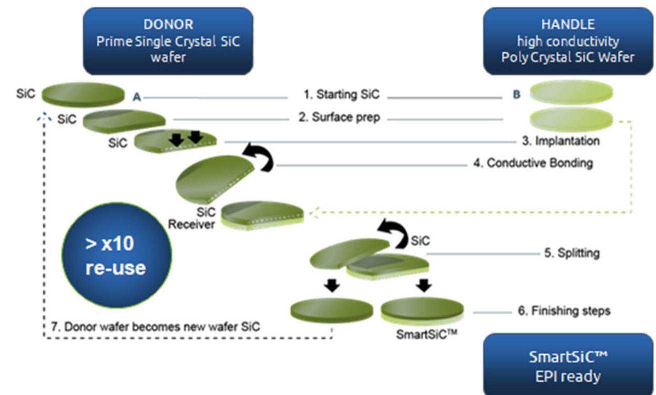

FIG. 1. SMART CUT™ TECHNOLOGY ADAPTED TO SILICON CARBIDE

INTRODUCTION

Silicon Carbide (SiC) technology in power electronics has become an essential enabler for advancing electric mobility and optimizing the utilization of renewable energy. As the demand in the market continues to rise, power semiconductor companies are pressed to urgently expand their capacity. Although there has been notable improvement in the quality and supply of 4H-SiC material, achieving low defect density wafers for high yields remains a challenge. In response to this, we have introduced a groundbreaking SiC engineered substrate. In September 2022, we inaugurated a dedicated manufacturing line [1] for the high volume manufacturing of this new product.

EXPERIMENTAL

The Smart Cut™ technology (see fig 1) enables the integration of high quality SiC layer transfer for device yield optimization, combined with a low resistivity handle wafer (<5mOhm.cm) to improve device conduction and switching losses [1-4] both for 150mm and 200mm wafers diameter (see fig 2). The SmartSiC™ engineered substrate is composed of a thin (between 350 and 800nm) high-quality 4H-SiC layer bonded (conductive bonding) on top of a 350µm thick polycrystalline SiC handle wafer.

The initial single crystal donor wafers can be re-used multiple times, leading to efficient usage of the SiC boule materials. Conventional wafering technology can extract a maximum of 50 wafers per boule, whereas our technology enables the preparation of up to 500 wafers out of the same boule.

Compared to standard single crystal 4H-SiC material with a conductivity around 20mΩ.cm, resistivities well below 5mΩ.cm are achieved (see Fig. 3) for polycrystalline SiC (pSiC) handle wafer.

FIG. 2. 150MM & 200MM SMARTSIC™ SUBSTRATE READY FOR SIC DRIFT EPITAXY

By means of a high material doping, the electrical resistivity of the pSiC substrate is reduced by a factor of at least 4, up to 10, compared to conventional single crystal SiC (mSiC) wafers. Less than 5 mOhm.cm electrical resistivity is guaranteed, with typical value in the range of 1 to 2 mOhm.cm. Through the application of CVD technology, the performance remains consistent across wafers for substrate diameters of both 150mm and 200mm. This consistency can be replicated using various

material sources, a crucial factor for industrial applications, as illustrated in figure 3.

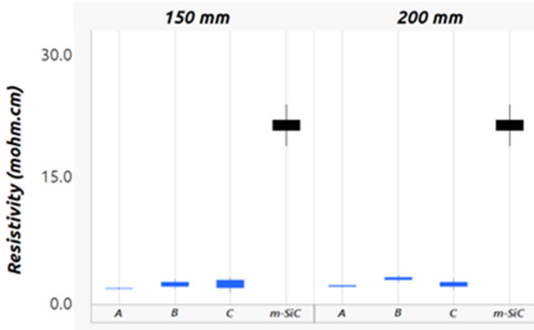

FIG. 3. ELECTRICAL RESISTIVITY DISTRIBUTION OF PSIC (A, B, C SOURCES) COMPARED TO MSIC SUBSTRATE.

Such a high electrical conductivity is confirmed from room temperature (25°C) to maximum device operating temperature (175°C) as stated on Table 1 which compares electrical resistivity on single crystal SiC, pSiC & SmartSiC™ wafer bonding interface over the whole temperature range [5].

Temperature	25°C	175°C
4H-SiC bulk [mOhm.cm]	15 – 25	15 – 25
Bonding Interface [mOhm.cm²]	0.003 – 0.006	0.002 – 0.006
Handle pSiC bulk [mOhm.cm]	1.5 – 2.2	1.7 – 2.5

TABLE 1: ELECTRICAL RESISTIVITY FOR EACH SMARTSIC LAYER, FROM 25°C TO 175°C

Polycrystalline SiC handle wafers are prepared through the chemical vapor deposition (CVD) technique. This process is much more energy-efficient than the conventional physical vapor transport (PVT) used to manufacture mSiC wafers, cutting CO_2 emissions of the final SmartSiC™ product by at least 70% compared to conventional single crystal SiC.

DEVICE EXPERIMENTAL CONDITIONS

The fabrication of 0.09mm² 1200V JBS diodes and MPS diodes (with areas of 2.5 and 6.12mm²: see figure 4) has been performed in collaboration with Fraunhofer IISB. In parallel 1200V SiC planar MOSFETs are also being fabricated.

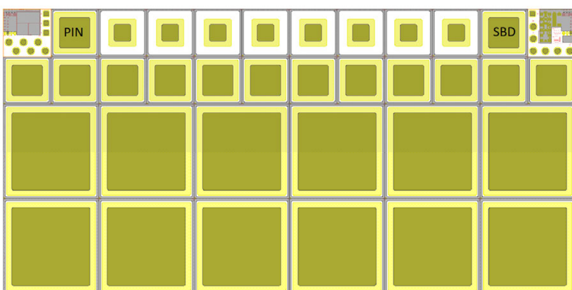

FIG. 4: TEST MASK FOR SIC DIODES FABRICATION.

Diode devices were fabricated with both commercial 150 mm 4H-SiC wafers and 150mm SmartSiC™ engineered substrate processed in parallel for both epitaxy and device fabrications. The drift layer is an n-type epitaxial layer of 11 µm thickness and $1 \cdot 10^{16}$ cm^{-3} doping concentration. This epitaxial layer is designed for a 1200 V blocking capability. The die thickness was reduced down to 340µm. The rated current ranges from 1A for 0.09mm² JBS diodes, 4A and 9A for respectively 1.6x1.6mm and 2.5x2.5mm MPS diodes. P+ doped layers are 500nm deep with a width of 2.5µm and 2.0µm respectively for JBS and MPS diodes.

For the front side metallization, we deposited (through evaporation) 80 nm Ti and 300 nm Al on the p+-regions and anneal via RTP. On top (and on the n-region) we sputtered the power metal – 50 nm Ti, 3500 nm Al and 20 nm Ti, which also builds the Schottky contact on the not-implanted epi.

For the back side metallization, we deposited (through sputtering) 60 nm $NiAl_{2.6\%}$ and use laser annealing on 4H-SiC to create the ohmic contact, on top of that we sputter 2000 nm Al and then evaporate the solder stack – 100 nm Cr, 1000 nm Ni and 1000 nm Ag. For the SmartSiC substrate, no laser annealing was performed.

RESULTS

For 1200V JBS diodes, we have performed wafer level 300x300µm dies forward (see fig.5) and reverse characteristics (see fig.6). No critical change in the reverse characteristics is observed. Forward characterization is showing forward voltage drop lowering at the rated voltage.

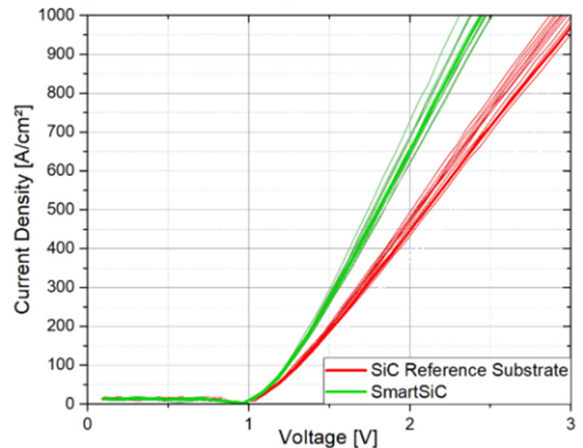

FIG. 5. FORWARD RESISTANCE OF RESPECTIVELY STANDARD SIC AND SMARTSIC™ FOR JBS DIODES.

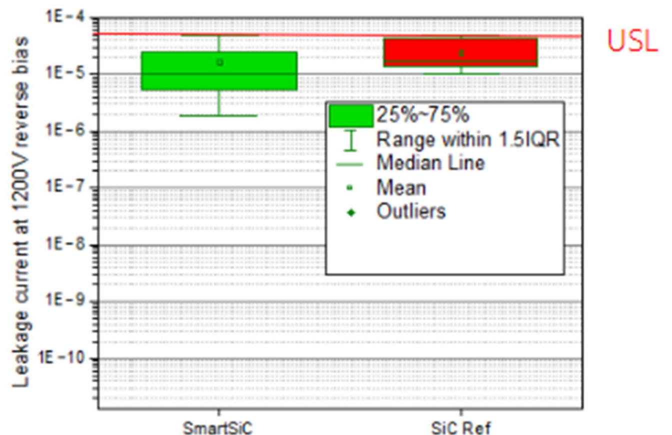

FIG. 6. REVERSE BIAS LEAKAGE AT 1200V OF RESPECTIVELY STANDARD SIC AND SMARTSIC™ FOR JBS DIODES.

For 1200V MPS diodes, we report wafer level dies forward characteristics. Voltage drop lowering at the respectively rated current of 4 and 9A for 1.6x1.6mm (see fig.7) and 2.5x2.5mm (see fig.8) MPS diodes, is around 12%. A first extraction of the dynamic on resistance of the forward regime (2

to 10A) of the MPS diodes leads to a benefit (linked to SmartSiC™ transition) around 0.9mOhm.cm². This is even beyond the expected gain linked to the improved material resistivity: around 0.77 mOhm.cm². This further gain is supposed to be linked to the lower contact resistance of the back side contact coming from the high level of doping in the pSiC [3].

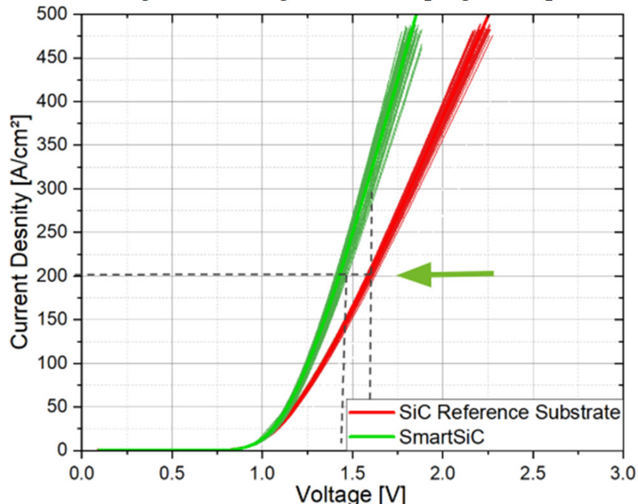

FIG. 7. FORWARD RESISTANCE OF STANDARD SIC AND SMARTSIC™ FOR 1.6x1.6mm 6A rated MPS DIODES.

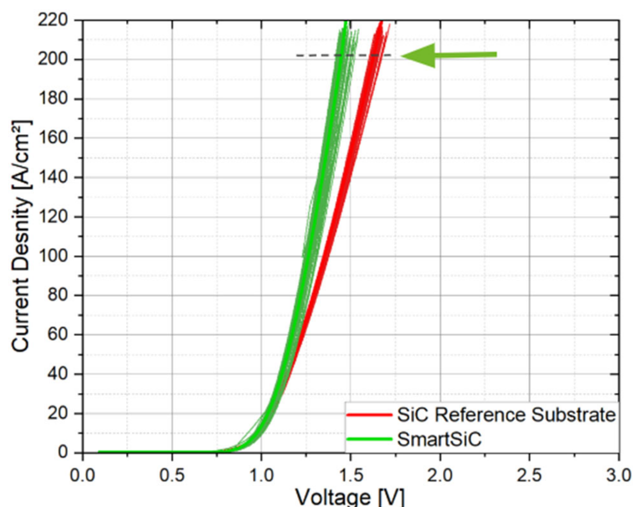

FIG. 8. FORWARD RESISTANCE OF STANDARD SIC AND SMARTSIC™ FOR 2.5x2.5mm 10A rated MPS DIODES.

Reverse I-V characteristics of SmartSiC™ based SiC diodes are shown in Fig.9 and 10 for respectively JBS and PIN diodes. Despite some device failures below the targeted voltage, the tested diodes reached the targeted voltage with a current leakage below the specifications. This is showing that SmartSiC™ engineered substrate is fully compatible with SiC power device fabrication and reaches the targeted device leakage levels.

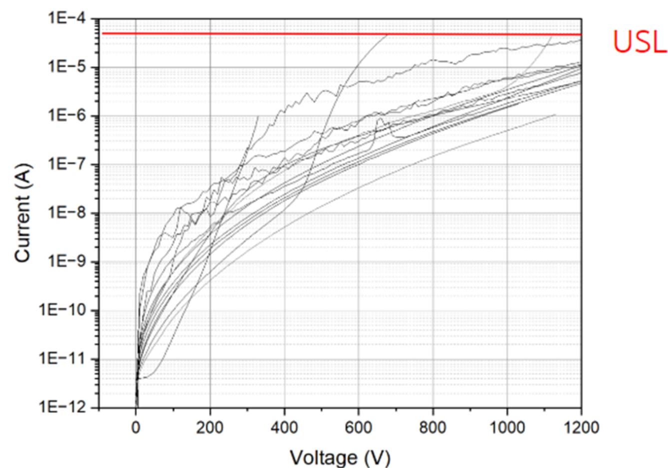

FIG. 9. REVERSE BIAS LEAKAGE OF SMARTSIC™ BASED JBS DIODES.

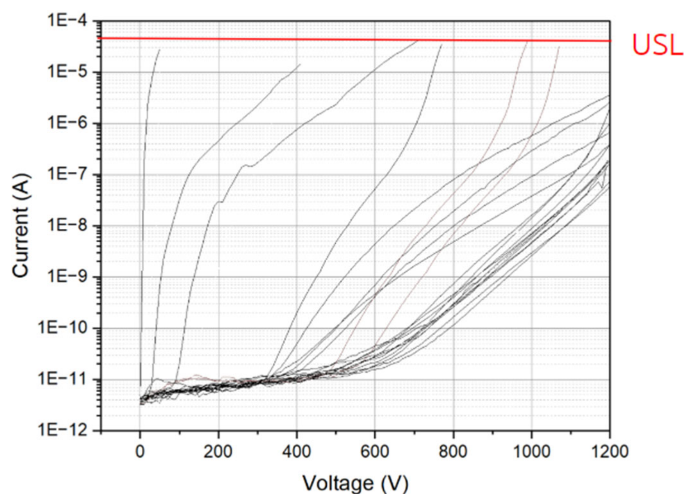

FIG. 10. REVERSE BIAS LEAKAGE OF SMARTSIC™ BASED PIN DIODES.

Perspectives for SiC MOSFETs performance

SmartSiC™ enables an increase of the current density at the device level thanks to both the polycrystalline SiC material's low resistivity and the lowered back side contact resistance. Compared to standard single crystal SiC substrate with a material electrical resistivity around 20mOhm.cm, the polycrystalline SiC material can reach material resistivity as low as 2mOhm.cm . In parallel, thanks to the high doping level of polycrystalline SiC, the contact resistance is lowered around 10-50 µOhm.cm². Associated with substrate selection and/or specific surface preparation prior to Smart Cut™ that will guarantee the best yield, the technology will enable a lowering of the total cost of ownership of power devices.

The benefit of the electrical parameters can be calculated as a function of device specific resistance (Ron.A) at room temperature and die thickness. We clearly see that for Ron.A improvement up to 15% for state of the art 1200V SiC MOSFETs and up to 18% for next generation 1200V SiC MOSFETs, can be envisioned (see fig.11). Considering ultimate SiC MOSFET or state of the art JFET, improvement up to 30% is anticipated.

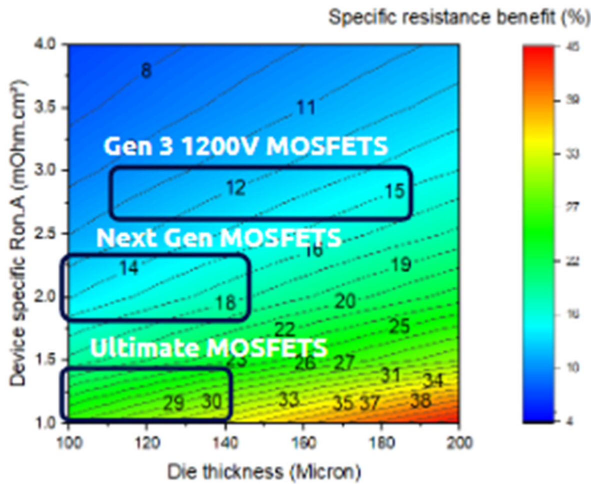

FIG. 11. RON.A BENEFIT ENABLED BY SMARTSIC™ USE FOR 1200V SIC MOSFET.

BIPOLAR DEGRADATION BENEFITS OF SMARTSIC™ MATERIAL

Bipolar degradation of post epitaxy SiC substrates without diode processing was carried out on reference and engineered SiC substrates using the E-V-C technique developed by ITES, Co. (Japan). This involves initiating bipolar degradation driven by SSF through UV illumination, followed by a focused examination of photoluminescence using a selective band-pass filter (BPF) at approximately 420 nm [6]. Different UV intensities with a wavelength of 355 nm were used (38, 75 and 150W/cm²).

As the UV illumination power increases, SSFs develop, with a rate 4 to 12 times faster in the case of single crystal SiC compared to SmartSiC™ (ratio of linear regression of SSF area over illumination between the 2 wafer designs). Fig. 12 provides a comparison of observation fields using the 420nm band-pass filter (BPF).

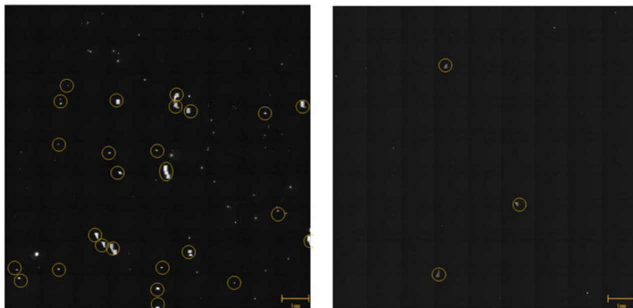

Fig. 12. Typical 10x10mm observation fields post UV illumination (here 150 W) 420nm BPF PL of bipolar degradation severity between bulk+epi (left) vs. SmartSiC™+epi (right).

The findings appear to validate the inherent asset of the SmartSiC™ design over bulk material in the context of robustness against bipolar degradation. This characteristic was previously assessed through a forward-current stress test conducted on 4H-SiC epitaxial layer subjected to proton irradiation [7]. In the present case, it appears that both the number of SSFs and their typical size are lower in the case of SmartSiC™ compared to bulk. Next step will be the assessment of MPS diodes and MOSFETs body diodes under current surge test conditions.

CONCLUSION

In conclusion, we are demonstrating that the SmartSiC™ engineered substrate solution available in 150 and 200mm diameters will bring a higher current density (up to 30%) both for state of the art SiC MPS diodes and MOSFETs (either planar or vertical). Besides modeling, SiC devices have been fabricated and diodes (JBS and MPS) with voltage drop improvement by 12% at rated current have been demonstrated. Finally we have demonstrated post epitaxy robustness with regards to bipolar degradation. This will be further assessed at device level.

ACKNOWLEDGEMENTS

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ACRONYMS

MPS	MERGED-PIN-SCHOTTKY
JBS	JUNCTION-BARRIER-SCHOTTKY
PIN	POSITIVE INTRINSIC NEGATIVE
PSIC	POLYCRYSTALLINE SILICON CARBIDE
MSIC	SINGLE CRYSTAL SILICON CARBIDE
IISB	INSTITUT FÜR INTEGRIERTE SYSTEME UND BAUELEMENTETECHNOLOGIE
SSF	SHOCKLEY STACKING FAULT
UV	ULTRA VIOLET
CVD	CHEMICAL VAPOR DEPOSITION
PL	PHOTOLUMINESCENCE