Design, Fabrication, and Characterization of GaN-Based Single Drift Region IMPATT Diodes

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Abstract

GaN-based single drift region impact-ionization avalanche transit-time (IMPATT) diodes have been designed, simulated, fabricated, and demonstrated experimentally. The breakdown voltage is measured to be 194 V, which is close to the simulated breakdown voltage of 196 V. The breakdown mechanism is verified to be avalanche breakdown by temperature dependent reverse-bias I-V measurement. On-wafer RF measurement showed that the diode has microwave-frequency reflection gain due to the onset of negative differential resistance between 10.9 GHz and 16.6 GHz. These devices are promising for high-power, high-efficiency microwave and millimeter-wave signal generation.

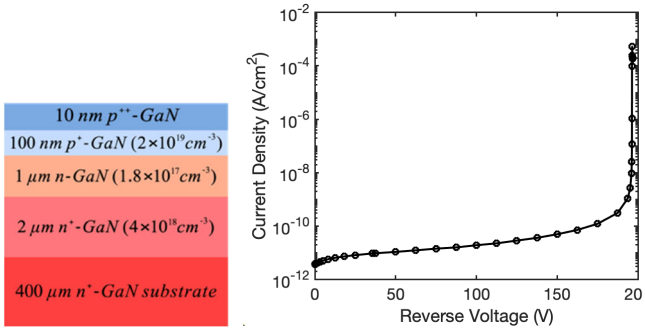
Introduction

IMPATT diodes offer very high power density and DC-to-RF conversion efficiency for microwave- and millimeter-wave frequency solid-state sources [1]. While IMPATT diodes based on Si and GaAs are well developed (see e.g. [2], [3], [4], [5]), compared with Si and GaAs, GaN has favorable material properties for high-frequency and high-power applications. In particular, the high carrier saturation velocity and higher critical electric field of GaN promises to significantly enhance the performance potential of GaN-based IMPATT diodes. Kawasaki et al. demonstrated the first operation of a GaN-based IMPATT [6], and recently demonstrated GaN single drift region (SDR) IMPATT diodes with oscillation frequency up to 21 GHz in a mechanically tuned resonant cavity [7].

While these results are very exciting as an initial demonstration of the technology, to better understand fundamental device physics, direct S-parameter measurement of IMPATT diodes is beneficial. However, due to measurement difficulties, very few papers on IMPATT diode S-parameter measurement have been published [8], [9]. In this paper, we demonstrate the first direct on-wafer S-parameter measurement of GaN IMPATT diodes that exhibit clear reflection gain. This was made possible by optimization of the fabrication process to suppress the leakage current sufficiently, as well as to optimize the measurement conditions to limit thermal effects. For low-parasitic RF measurements, both the anode and cathode pads are placed on the top of the wafer, enabling the use of on-wafer probes. The measured GaN SDR IMPATT diode showed gain between 10.9 GHz and 16.6 GHz, with a peak reflection gain of 0.17 dB at 13.6 GHz.

Device Design and Simulation

Fig. 1 (a) shows the schematic of the designed GaN SDR IMPATT diode structure. The structure consists of 10 nm of p^{++}-GaN, 100 nm of p^{+}-GaN ([Mg]: $2 \times 10^{19} cm^{-3}$), a 1 μm n-GaN drift layer ([Si]: $1.8 \times 10^{17} cm^{-3}$), a 2 μm n^{+}-GaN contact layer ([Si]: $4 \times 10^{18} cm^{-3}$), on a 400 μm thick n^{+}-GaN substrate. Sentaurus TCAD simulation is performed to predict breakdown voltage. The impact ionization coefficients for GaN were based on our group's previous work [10]. Fig. 1(b) shows the simulated I-V curve of the diode, with a projected breakdown voltage of 196 V.



(a) (b)

Fig. 1. (a) Schematic of simulated GaN SDR IMPATT diode. (b) I-V curve of the simulated SDR IMPATT diode. The breakdown voltage is around 196V.

Fabrication Process

The fabricated device has the same epitaxial structure as the simulated diode in Fig. 1. A schematic cross-sectional diagram, a top-view optical image of a completed device, and an oblique-view SEM of a fabricated device are shown in Fig. 2. For simplicity of probing with low parasitics despite the n+ substrate, the n-type cathode contacts were probed directly with the grounds of the GSG on-wafer probes, with the central anode contact in contact with the signal line of the probe. The mesa structure was fabricated in inductively coupled plasma-reactive ion etching (ICP-RIE) with 100 nm of Ni as the mask. The etch depth is targeted at 2 μm so that the etch floor is well within the n^{+}-GaN cathode contact layer. Vertical sidewalls

with acceptable damage were achieved by an optimized Cl_2-based etch recipe. The plasma self-bias voltage was kept low, at approximately 70 V, to minimize sidewall damage.

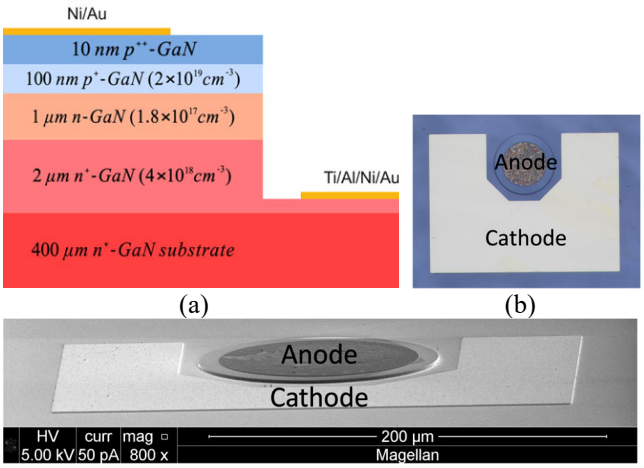


Fig. 2. (a) Schematic diagram, (b) optical image, and (c) oblique SEM of a fabricated device.

As was reported in other studies, the type of carrier wafer has a great impact on the etch floor due to different etch by-products generated by the carrier wafer. [11], [12]. Severe micro-masking effects were observed with SiO_2 and sapphire carrier wafers. This poor etch morphology is particularly detrimental for our devices with relatively high etch depth of 2 μm. Fig. 3 (a) shows a typical etch floor with SiO_2 carrier wafer. Needle-like nanostructures are formed on the etch floor possibly due to non-volatile etch by-products. Using a Si carrier wafer was found to avoid micro-masking and rough surfaces (see Fig. 3(b)). After etching, the sample was treated with 25% TMAH at 85 °C for 45 minutes to remove damaged GaN around the periphery of the mesa and make the sidewalls more vertical. The Ni mask was removed in HF:H_2O_2:H_2O = 1:1:20. An etched test sample after TMAH treatment and Ni mask removal is shown in Fig. 3 (b). It can be seen that the sidewalls are smooth and vertical, and the etched floor is clean and smooth.

After Ni mask removal, p-contact (Ni/Au 30/200 nm) and n-contact (Ti/Al/Ni/Au 30/100/50/200 nm) metals were deposited by electron beam evaporation and lift-off. The n-contact metals were deposited on the front side (on the etch floor) to facilitate RF probing. The p-contact was annealed at 515 °C for 10 minutes in air using an AccuThermo AW610 rapid thermal processor. Finally, 12 nm of ALD Al_2O_3 was deposited to passivate the mesa sidewalls and further reduce leakage current.

CHARACTERIZATION

The fabricated devices were characterized at DC and RF. Fig. 4. shows the temperature dependent reverse I-V measurement of a typical device. The breakdown voltage at 25 °C is 194 V, which is close to simulation predictions (196 V). As temperature increases from 25 °C to 75 °C, the break-

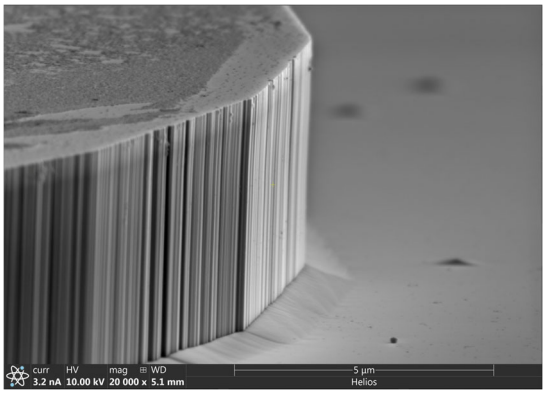


Fig. 3. SEM image of etched test sample. (a) Etched with SiO_2 carrier wafer. The etched floor has needle-like nanostructures and further etching is prevented. (b). Clean and smooth etched floor with Si carrier wafer. The sidewalls are vertical and smooth after TMAH treatment.

down voltage increases. This is a sign of avalanche breakdown. The temperature coefficient is calculated to be 0.28 V/K.

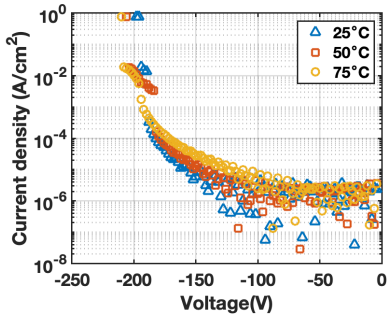


Fig. 4. Temperature dependent reserve bias I-V measurement. The breakdown voltage is higher at higher temperatures.

Small signal RF measurements under pulsed conditions were used to assess the RF behavior of the devices. A schematic of the measurement system is shown in Fig. 5. To minimize self-heating during the measurements, pulsed bias voltage was used, using an Auriga AU-5 pulse head that was

modified to enable negative voltage pulsing. Pulse voltages up to -200 V with pulse width of 400 ns and repetition rate of 4 ms were used for a duty cycle of 0.1 %. A high-voltage, wide band bias tee/diplexer was used to allow the use of large pulsed biases without ringing. For S-parameter measurements, a Keysight PNA-X N5247B was used that can measure from 10 MHz to 67 GHz. The system was calibrated to the probe tips with an off-wafer impedance standard substrate (ISS). The calibrated s-parameters, without additional de-embedding, are reported here since the device contacts are directly on the active region of the device without distinct pad structures.

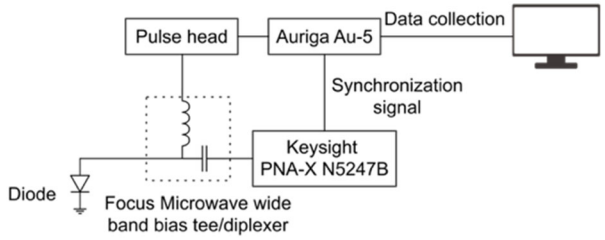
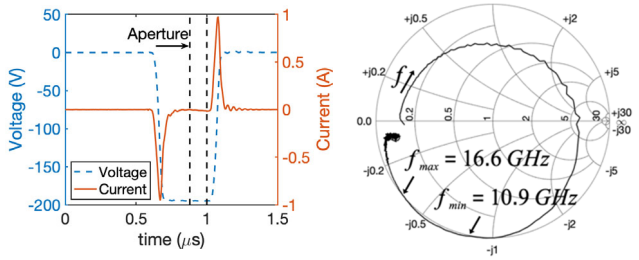


Fig. 5. Schematic of pulsed small signal RF measurement system.

Fig. 6 (a) shows the typical input voltage and current waveform measured by Auriga AU-5. Two large spikes, at the rising and falling edge of voltage pulses, are due to displacement current that is caused by charging and discharging of the junction capacitance. As is shown in Fig. 6 (a), the time aperture window for RF measurement is set to be narrow and close to the end of the pulse (0.88 μs to 1 μs throughout the measurement) so that the displacement current does not influence the S-parameter measurement. A typical RF measurement of the reflection coefficient (Γ) from 100 MHz to 67 GHz is shown in Fig. 6 (b), corresponding to a bias of -200 V. As can be seen, the device is passive at low frequencies, leaving the unity Smith chart between 10.9 GHz and 16.6 GHz. A peak reflection gain of 0.17 dB is found at 13.6 GHz.



(a) (b)

Fig. 6. (a) Input voltage and current waveform with pulse bias voltage of – 200 V. (b) Smith chart plot of RF measurement result from 100 MHz to 67 GHz with pulse bias voltage of -200 V.

Fig. 7 shows the measured reflection coefficient magnitude of a typical 120 µm diameter device for several different pulsed reverse bias voltages. The peak of the reflection coefficient increases as the pulsed reverse bias voltage (current density) increases, and the frequency of the peak gain also increases with bias. This is consistent with expectations from theory for IMPATT diodes [13]. Further increasing bias voltage is expected to further shift reflection gain to higher frequencies but this is limited by the capability of our pulse system.

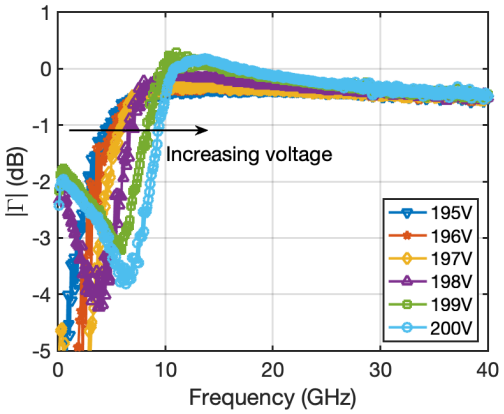


Fig. 7. Magnitude of reflection coefficients at different pulsed reverse bias voltages.

Conclusions

A GaN SDR IMPATT diode has been designed, simulated, fabricated, and characterized. The breakdown voltage is measured to be 194 V and is close to the simulated breakdown voltage of 196 V. Temperature dependent reverse I-V measurement verifies avalanche breakdown, and the temperature coefficient is 0.28 V/K. Small signal RF measurements show that the diode has gain up to 16.6 GHz and has a peak gain of 0.17 dB at 13.6 GHz. To the authors' knowledge, this is the first report of directly-measured reflection gain in a GaN-based IMPATT diode.

Acknowledgements

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