High Temperature Operation of GaN High Electron Mobility Transistors on Large-Area Engineered Substrates for Extreme Environments

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Abstract

Gallium nitride (GaN) high electron mobility transistors (HEMTs) were fabricated on coefficient of thermal expansion (CTE)-matched large-area (200 mm) engineered substrates with 5 µm thick buffer layers. Temperature dependent electrical characterization, including DC output, DC transfer, and pulsed output characterization, was performed from room temperature up to 600 °C. From DC output characterization, ON-resistance increased with temperature, and the maximum drain current, I_{max}, at V_{GS} = 2 V, V_{DS} = 10 V decreased 72% as temperature was increased from room temperature to 601 °C. High temperature operation (601 °C) also lead to increased OFF-state leakage which reduced the ON/OFF ratio from ~10^4 at room temperature to ~10^2 at 601 °C. Pulsed output characteristics with quiescent gate and drain biases V_{GSQ} = -5 V and V_{DSQ} = 30 V showed that ON-resistance initially increased from room temperature up to 400 °C; as the stage temperature was further increased, this trend reversed and ON-resistance began decreasing. Additional pulsed output characterization was performed with various gate and drain quiescent biases. At lower temperatures (206 °C), significant current collapse was observed as the quiescent drain bias was increased for a constant V_{GSQ} = -5 V; however, at high temperature (584 °C), current collapse reduced significantly. As V_{DSQ} was increased from 10 V to 30 V (with V_{GSQ} = - 5 V), there was no change in ON-resistance or I_{max} at 584 °C.

Introduction

The wide bandgap (~3.4 eV) and high mobility of GaN make it an ideal candidate for a multitude of RF and power electronics applications. Additionally, AlGaN/GaN heterostructures can be grown to form a two-dimensional electron gas (2DEG) below the heterointerface with very high room temperature mobility (>2000 $cm^2V^{-1}s^{-1}$). While the wide bandgap of GaN is enticing for higher breakdown strength, it is also promising for high temperature operation in extreme environments such as deep-well drilling, aviation, and hypersonics. However, performance degradation and thermal stress can lead to reliability concerns or failure. Qromis Substrate Technology (QST™) substrates with a polycrystalline AlN core have been designed to be coefficient of thermal expansion (CTE)-matched to GaN to enable the growth of thick buffer layers on large diameter (150, 200, 300 mm) substrates with minimal residual stress. [1] This could potentially enable improved device performance and reliability in high temperature environments as compared to traditional substrate choices (e.g. Si, SiC, and sapphire).

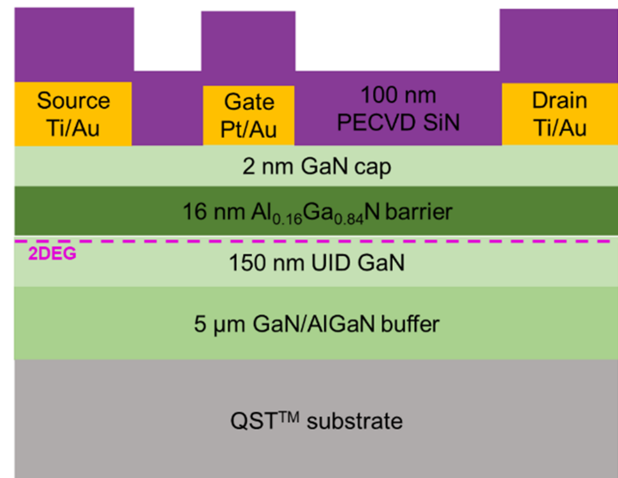


Fig. 1. Cross-sectional schematic of the GaN HEMT measured in this study.

Experimental

GaN high electron mobility transistors (HEMTs) were fabricated on QST substrates with GaN/AlGaN buffer thicknesses of 5 µm (Fig. 1). The epitaxial stack was grown using metal organic chemical vapor deposition (MOCVD); details are provided in Fig. 1(b). Schottky gate (Ni/Au) and Ohmic contacts (Ti/Al/Ni/Au) were deposited via e-beam evaporation, and Ohmic contacts were alloyed via rapid thermal annealing (850 °C, 30 s, in N_2). Devices were passivated with 100 nm thick SiN deposited via plasma-enhanced CVD (PECVD).

The sample surface temperature was calibrated using an on-wafer resistance temperature detector (RTD) test structure; the RTD test structure was fabricated on both sapphire and silicon wafers (Fig. 2) to assess the impact of substrate thermal conductivity on the sample surface temperature. High temperature device operation was performed in a MicroXact probe station under vacuum (≈10^{-3} Torr). Electrical characterization was performed using a Keithley 4200SCS semiconductor parameter analyzer.

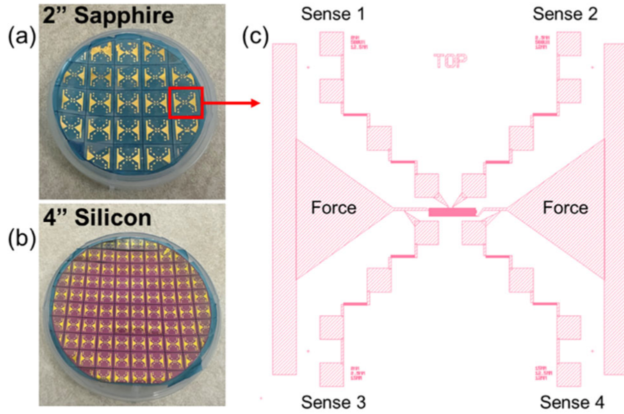


Figure 2. Test structures for stage temperature calibration on (a) 2" sapphire and (b) 4" silicon wafers. (c) Plan-view schematic of the test structure used for stage temperature calibration.

Results and Discussion

Fig. 3 shows temperature dependent DC output and transfer characteristics of the GaN-on-QST HEMT from room temperature to 600 °C. As temperature increased, I_{max} (at $V_{GS,max}$=2V) decreased 72% from 21 mA at RT to 5.9 mA at 601 °C. From the slope of the DC output characteristics in the linear regime, the expected increase in R_{ON} with temperature is observed, as well as a walkout of the knee voltage. [2]

From the DC transfer characteristics (Fig. 3(b)), the OFF-state leakage current held relatively constant from RT to 203 °C, but increased an order of magnitude with each additional 200 °C increase in temperature. Between the increase in OFF-state leakage and decrease in ON-state current, the ON/OFF ratio reduced from >10^4 at RT to <10^2 at 601 °C. As shown in Fig. 3(c), the increase in OFF-state leakage was due to gate leakage at high temperature.

In addition to DC electrical characterization, temperature dependent pulsed device characteristics of the GaN HEMTs were measured. Quiescent gate-source and drain-source biases ([V_{GSQ}, V_{DSQ}]) of [0, 0], [-5, 0], [-5, 10], [-5, 20], and [-5, 30] V were used. Fig. 4. shows the temperature dependence of the pulsed output characteristics for the harshest quiescent point of [V_{GSQ} V_{DSQ}] = [-5, 30] V with a measurement gate voltage of 0 V. As temperature is increased from room temperature (23 °C) to 400 °C, there is a large increase in the ON-resistance and the maximum drain current density (I_{max}) decreases. This is to be expected as the higher

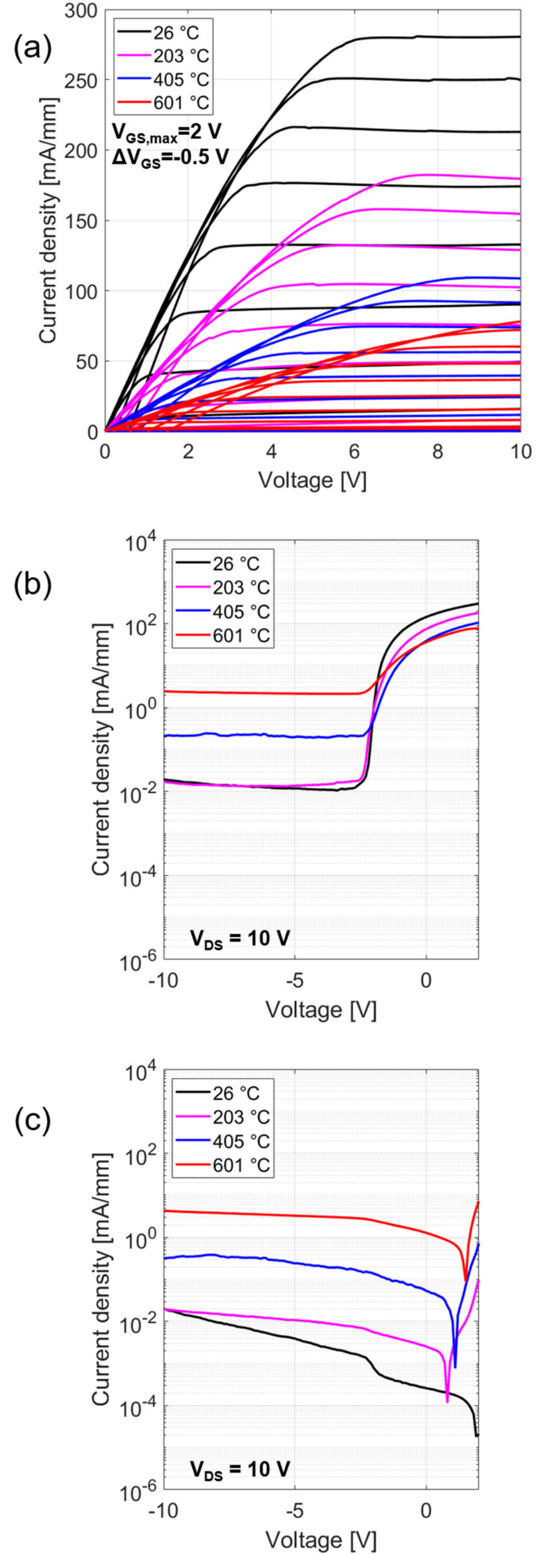


Fig. 3. Temperature dependent (a) DC output and (b),(c) DC transfer characteristics of the GaN HEMT with 5 µm buffer thickness (QST5). Both (b) drain and (c) gate current are shown as a function of V_{GS}.

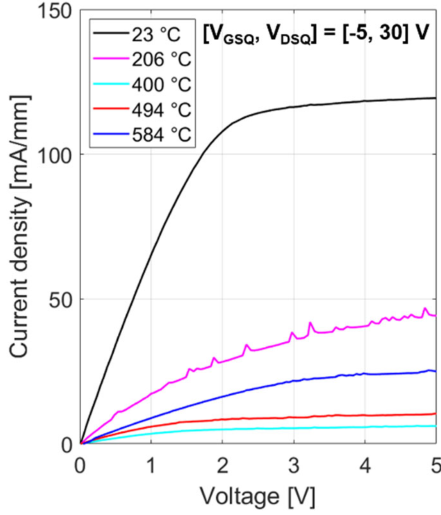


Fig. 4. Temperature dependent pulsed output characteristics (I_d-V_{ds}) with a quiescent gate bias of -5 V and a quiescent drain-source voltage of 30 V. The gate bias during measurement is V_{GS} = 0 V.

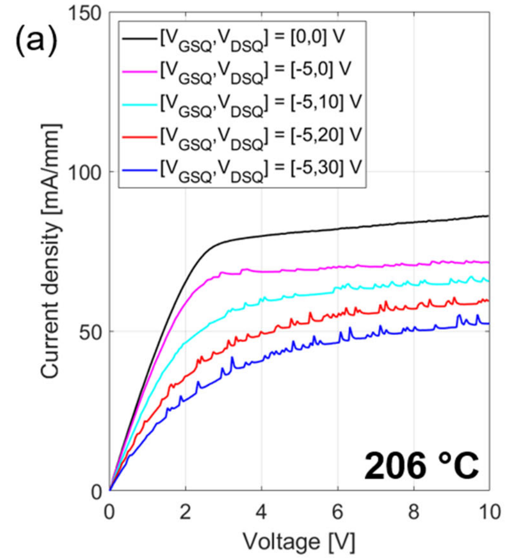
operating temperature will lead to more electron-phonon scattering and lower the carrier mobility. However, as temperature is further increased to 494 °C and 584 °C, the ON-resistance is observed to recover and begins to increase, which is accompanied by increasing I_{max}.

Fig. 5 shows pulsed output characteristics as a function of quiescent bias at stage temperatures of 206 °C (Fig. 5(a)) and 584 °C (Fig. 5(b)). At lower temperatures, such as 206 °C, current collapse is observed and increases as the quiescent bias conditions become harsher (i.e., more negative quiescent gate bias and more positive quiescent drain bias). From [V_{GSQ}, V_{DSQ}] = [0, 0] V to [-5, 30 V], I_{max} decreases ~40%.

When temperature is increased to 584 °C, I_{max} decreases for a given quiescent bias condition as was observed in Fig. 4. However, the drain current dispersion behavior changes drastically. Initially, there is still a slight reduction in I_{max} and an increase in ON-resistance as the quiescent bias becomes harsher. In contrast with lower temperatures, once the quiescent bias reaches [V_{GSQ}, V_{DSQ}] = [-5, 10] V, no further current collapse is observed as the quiescent bias becomes harsher. Measurements of the gate current (not shown) under these pulsed bias conditions at 584 °C revealed that gate leakage was still two orders of magnitude smaller than the drain current density and is not responsible for the apparent loss of current collapse.

Conclusions

In conclusion, GaN HEMTs were fabricated with 5 µm thick buffer layers on CTE-matched engineered QST structures. Temperature dependent electrical characterization was performed under both DC and pulsed bias conditions up to temperatures of 600 °C. Under DC bias, OFF-state leakage remained relatively constant up to 200 °C, after which leakage increased ~10X for each additional 200 °C increase in



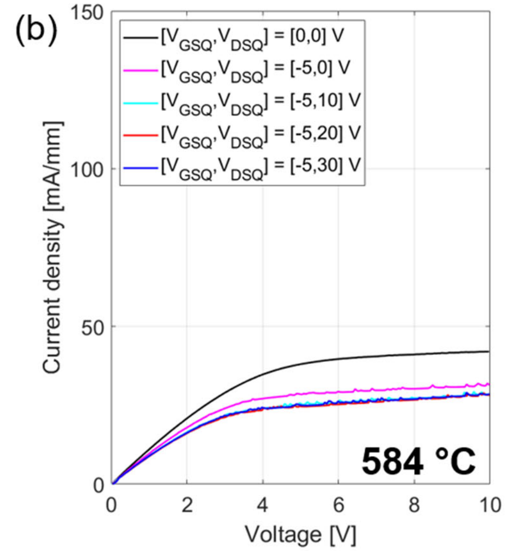


Fig. 5. Pulsed output characteristics (I_d-V_{ds}) with quiescent biases of [V_{GSQ}, V_{DSQ}] = [0, 0], [-5, 0], [-5, 10], [-5 20], [-5, 30] V. Pulsed output characteristics were measured with stage temperatures of (a) 206 °C and (b) 584 °C. The gate bias during measurement is V_{GS} = 0 V.

temperature. At 600 °C, I_{max} decreased 72% at $V_{GS,max}$ = 2 V as compared to room temperature. Under pulsed bias conditions with quiescent bias of [V_{GSQ}, V_{DSQ}] = [-5, 30] V, ON-resistance increased and I_{max} initially decreased as temperature was increased. However, at temperature was increased above 400 °C, I_{max} recovered and ON-resistance began decreasing. Additionally, at high temperatures (584 °C), current collapse effects significantly decreased and no change in I_{max} or ON-resistance was observed for pulsed bias characteristics with quiescent biases of [V_{GSQ}, V_{DSQ}] = [-5, 10] V, [-5, 20] V, and [-5, 30] V. The mechanism for the observations of reduced/no current collapse and recovery of

I_{max} and ON-resistance at higher temperatures is currently under investigation. This work is significant for studying device physics, benchmarking performance, and investigating reliability concerns of GaN HEMTs operating in extreme environments for high temperature applications.

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