QuickSELs Enabling Rapid Feedback to Epitaxy

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Abstract

Quick VCSELs (QuickSELs) which reduce processing time to under 24 hours whilst minimising impact on device performance have been developed with applications in product development and quality control in commercial VCSEL production. A comprehensive assessment of the QuickSEL is given here, along with subsequent characterisation techniques which enable the assessment of large diameter epitaxial wafers.

Introduction

Vertical-cavity surface-emitting lasers (VCSELs) are today ubiquitous in modern technology findng use in computer mice, laser printers, short-reach data communications, 3D imaging, time-of-flight (ToF) sensors, miniature atomic clocks (MACs), industrial heating, and light detection and ranging (LiDAR) [1]. The requirements of the VCSEL vary widely in each case and, as such, so do the specific architectures of the final device. The foundation for the production of reliable, reproducible, high-performance VCSEL devices begins with the design and growth of the epitaxial structure. In the product development cycle, it is common for there to be systematic and iterative studies to optimise epitaxial designs and reactor conditions, as first outlined in [2]. In such a situation, it is crucial to have reliable methods for assessing material quality. Routine wafer characterisation methods include reflectance mapping, photoluminescence (PL), defect scanning, x-ray diffraction (XRD), and electrochemical capacitance-voltage (ECV) measurements. Of these, reflectance mapping, defect scanning, and XRD are non-destructive and can be carried out with a relatively high throughput. Destructive techniques, however, can only be carried out on sacrificial wafers. This means that quantitative analysis of the quantum well active layers (via PL) can only occur periodically.

These material characterisation methods must also be complemented by assessing the performance of working VCSEL devices. However, in order to minimise both time and financial cost, the fabrication and testing of these devices needs to be done on short timescales to enable rapid feedback to epitaxy. For that purpose, a stripped-back Quick VCSEL (QuickSEL) device design and fabrication process has been developed at Cardiff University and has since become a routine commercial service offered by the Institute for Compound Semiconductors (ICS). The QuickSEL design reduces the total processing time to under 24 hours whilst minimising the impact on device performance. Here, a comprehensive overview of QuickSELs are given, including the subsequent characterisation techniques which are used for the assessment of epitaxial material quality and uniformity.

QuickSELs

The principle of the QuickSEL is to significantly reduce processing time whilst preserving device performance. Relative to a standard structure, QuickSELs require no planarisation due to the atypical mesa etch geometries employed. Instead, selective oxidation of a buried high-Al layer forms both the VCSEL aperture and an electrically isolated probing/bond pad region. This can be seen in Fig. 1.

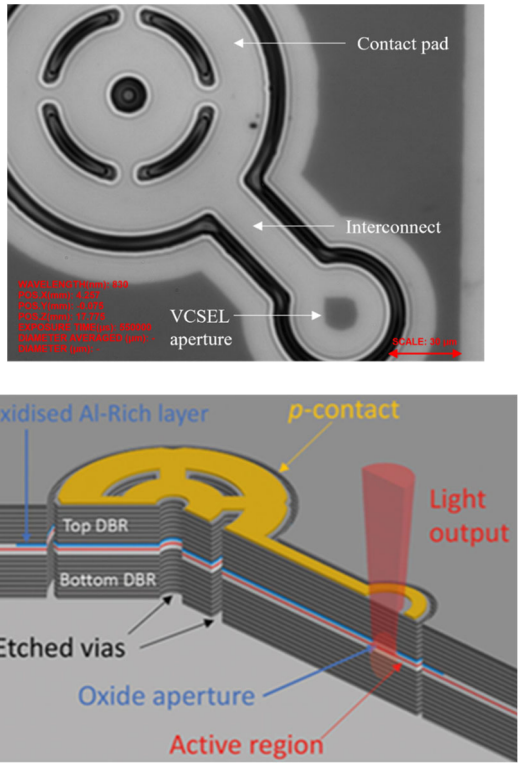

Fig. 1: QuickSEL device geometry; (top) optical image of fully processed QuickSEL (from [1]); (bottom) cross-sectional diagram showing key features of a QuickSEL. Courtesy of Dr. Richard Forrest.

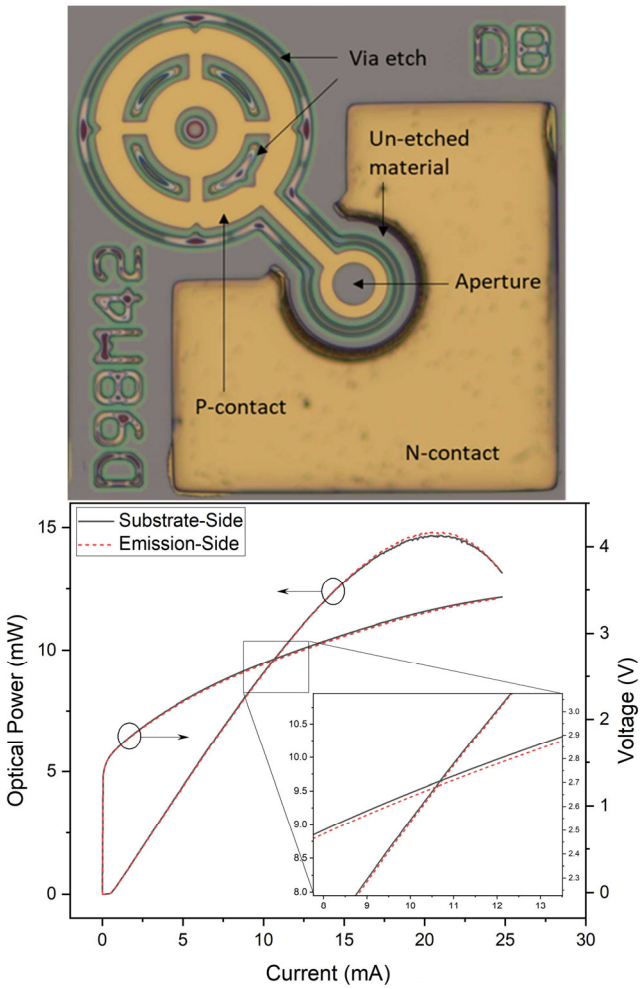

Fig. 2: co-planar electrode configuration designed to accommodate epitaxial structures grown on semi-insulating substrates (top) and P-I-V comparison of substrate- and emission-side contact configurations (bottom). Images from J. Baker (2023), PhD Thesis.

The device design is also adjusted to account for a range of epitaxial structures, for example, those grown with an anti-phase cap layer or those grown on semi-insulating substrates. For anti-phase material, the process begins with a $\lambda/4$ depth etch into the top DBR which defines an in-phase region.

In the case of growth on semi-insulating substrates, an extra etch step is included to facilitate a co-planar electrode configuration as shown in Fig. 2 (top). The resulting raw P-I-V data for a QuickSEL device processed with both a substrate- and emission-side n-contact is shown in Fig. 2 (bottom). In this case the growth substrate was n+ GaAs. This was done to assess the performance of QuickSELs with a co-planar contact arrangement. It can be seen that no significant degradation in device performance occurs for an emission-side n-contact relative to the global substrate-side n-contact and, hence, it is still possible to extract representative information.

With these adjustments, QuickSELs can be processed across wafers designed for high-frequency modulation bandwidths as well as those designed for single-frequency quantum-sensing applications. The different device variations discussed are diagrammatised in Fig. 3 and the corresponding processing times are detailed in Table 1.

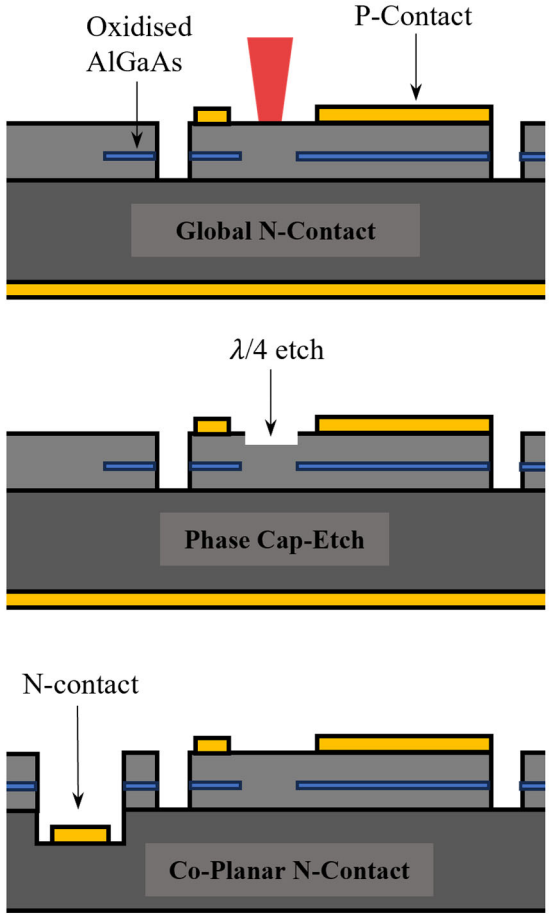

Fig. 3: Cross-sectional diagrams of QuickSEL device variations. Global n-contact structure (top) with the Al-oxide layer and p-contact layers labelled; phase cap-etch structure (middle) with the $\lambda/4$ etch within the VCSEL aperture labelled; and co-planar n-contact structure (bottom) with the n-contact labelled.

Table 1: QuickSEL device variations and processing times.

Device	Processing Time (Hours)
Global N-Contact	24
Phase Cap-Etch	28
Co-Planar N-Contact	30

WAFER-SCALE ANALYSIS

The Translational Research Hub at Cardiff University features a 1350 m^2 cleanroom operated by the Institute for Compound Semiconductors (ICS). This enables the bridging of the gap between research and volume production (processing wafers of up to 8-inch diameter). These facilities feature state-of-the-art 8-inch capable tools, including a Raith

EBPG5200 Plus e-beam; Heidelberg MLA-150 maskless aligner; A Suss MA8 contact mask aligner; Oxford Instruments and KLA (SPTS) plasma tools for dielectric deposition and dry-etching of III-Vs; Lesker Pro Line PVD 200 mm thin film deposition system and backend tools for automatic wafer thinning, cleaving and die pick-and-place. The facility is geared towards processing III-V optoelectronic chips and photonic integrated circuits, providing the ability to scale processes to 200 mm diameter wafers. Recently secured equipment also includes a new state-of-the-art oxidation furnace from Aloxtec, capable of handling wafers up to 8-inch and a Thermo-Fisher Helios 5 focussed ion beam scanning electron microscope (FIB-SEM).

To assess material quality, uniformity, and yield, the performance of processed QuickSEL devices is mapped across a wafer. The setup used for wafer-mapping is shown in Fig. 4. An MPI semi-automated probe-station is equipped with an integrating sphere which is connected to a Newport 1936-R calibrated power meter to facilitate true optical power measurements. An optical fibre is tapped from the integrating sphere and coupled to an Ocean Insight/ANDOR spectrometer with capability of obtaining high-resolution emission spectra with integration times < 1 s. The QuickSELs are typically driven CW using a Keysight B2910BL precision source/measure unit, which also supports four-terminal voltage measurements. Devices can also be operated pulsed using a Keithley 2520 pulsed laser diode test system. The chuck on which the wafers are mounted is temperature-controlled up to 200°C, although typically QuickSEL devices are measured up to 75 – 85°C. Electrical contact is made by direct probing with 2/7 μm footprint tungsten needle probe tips. The characterisation and mapping of device performance using this experimental setup provides valuable information used to quantify epitaxial material quality and uniformity.

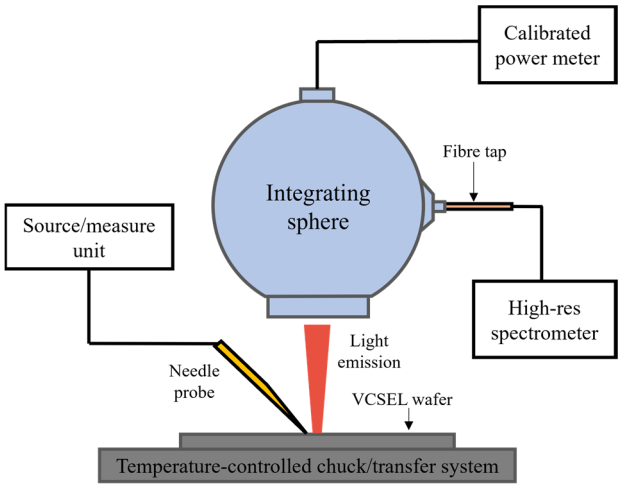

Fig. 4: Semi-automated probe station used for wafer-scale device characterisation. Adapted from [3].

An example wafer-map of threshold current density for 8 μm aperture QuickSELs across a 6-inch wafer designed for 940 nm sensing applications is shown in Fig. 5. Despite a uniform oxidation depth across the wafer, a centre-to-edge decrease in J_{th} is observed. By measuring the temperature dependence of threshold current, the decrease is found to be related to the detuning of the gain peak and cavity mode wavelengths. This is shown explicitly in Fig. 6 and reveals that the gain peak and cavity mode wavelengths are aligned at the edge of the wafer, leading to operation close to the threshold current minimum. Conversely, at the centre of the wafer the cavity mode is detuned on the long wavelength side of the gain spectrum, which means that operation at the threshold current minimum occurs at higher temperatures (close to 50 °C in this case).

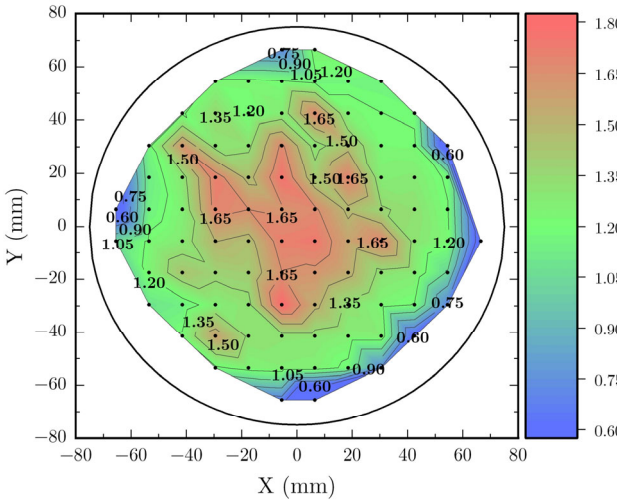

Fig. 5: Wafer map of peak optical power resulting from the characterisation of 5 μm aperture QuickSEL devices across a 6-

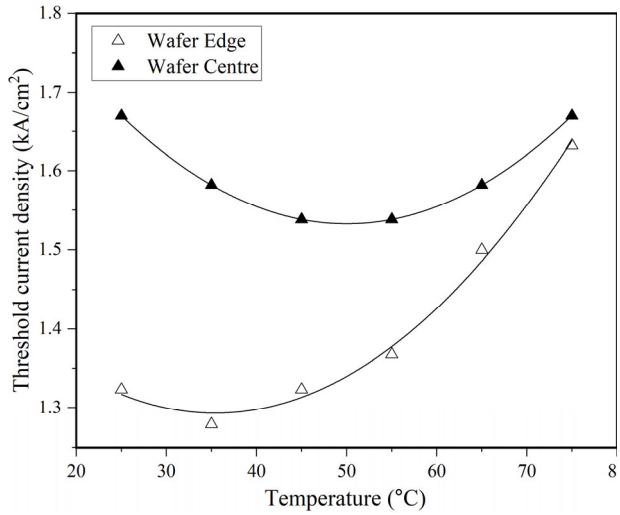

Fig. 6: Temperature dependence of threshold current density for approx. 8 μm oxide aperture QuickSEL devices measured at the centre and edge of a 6-inch wafer.

Ultimately, this centre-to-edge variation in detuning is the result of a difference in sensitivity to variation between the quantum well confined state energies (determined by the thickness, composition, and strain of the MQW) and the optical path length of the vertical cavity (determined by the thickness and composition of the inner cavity layers). Such information is invaluable for feedback to epitaxy whereby growth conditions can be optimised to reduce wafer-scale variation, in this case, adjusting the target Fabry-Perot dip/PL peak wavelengths. Furthermore, given that the relationship between the PL and gain peak wavelengths is non-trivial, temperature dependent measurement of threshold current is often the only viable method to gather this information. The QuickSEL allows the time-to-result for this kind of data collection to be minimised, which is highly advantageous both in the early stages of VCSEL product development and in routine quality control in volume production. This approach has since been applied in the development of VCSELs for atomic sensing applications and in DOE studies examining the use of germanium as a drop-in replacement growth substrate for volume production [3], [4], [5].

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ACRONYMS

VCSEL: Vertical-cavity surface-emitting laser
QuickSEL: Quick VCSEL
MAC: Miniature atomic clock
ToF: Time-of-flight
LiDAR: Light detection and ranging
PL: Photoluminescence
XRD: X-ray diffraction
ECV: Electrochemical capacitance-voltage
ICS: Institute for Compound Semiconductors
DBR: Distributed Bragg Reflector
DOE: Design of Experiment