The Effect of Operating Temperature on the On-State Performance of Quasi-Vertical Gallium Nitride MOSFETs

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Abstract – Vertical GaN MOSFETs are a promising technology for next generation efficient power systems. Here we investigate the effect of operating temperature on the on-state performance of quasi-vertical GaN MOSFETs, fabricated on SiC substrates. The threshold voltage, transconductance and on-resistance were extracted from measured characteristics across a range of temperatures. Shifts in both threshold voltage and transconductance are attributed to temperature dependent trapping-detrapping at the MOS interface. These are discussed in relation to series resistance contributions in the channel, drift layer and access resistances at the source and drain contacts.

INTRODUCTION

Gallium nitride (GaN) vertical devices have garnered significant interest within the power device community due to their ability to scale breakdown voltage independently of chip area. This offers a route to scale GaN-based solutions to voltage ranges beyond those offered by current commercial HEMT devices. Unlike lateral devices, vertical GaN MOSFETs direct electric fields away from the surface, thereby addressing reliability concerns and mitigating dielectric breakdown issues associated with elevated surface fields. Some of the key barriers to the commercialization of vertical GaN technologies are (1) high cost, limited availability and quality of native substrates (2) difficulties in growing high quality epitaxy on foreign substrates and (3) thermal management due to the lower thermal conductivity of GaN compared with e.g. silicon carbide (SiC) [1]. In addition, the GaN MOS interface has received relatively little attention compared with SiC and is not yet well understood or fully optimized [2, 3]. Here we investigate the on-state performance of GaN-on-SiC quasi-vertical MOSFET devices at elevated temperatures, typical of those encountered under device operation. These devices are used to demonstrate how series resistance contributions may be extracted as a function of temperature, and the relative contribution of these components to total conduction losses is discussed.

DEVICE FABRICATION AND TESTING

The GaN epitaxy was grown on 100mm semi-insulating 4H-SiC wafers via MOCVD. A 60nm AlN layer was used for nucleation, followed by a 500nm N^+-GaN drain layer (Si, $1 \times 10^{19} \mathrm{cm}^{-3}$), a 2.5µm N^--GaN drift layer (Si, $1 \times 10^{17} \mathrm{cm}^{-3}$), a 400nm Mg doped P-GaN layer (Mg, $3 \times 10^{19} \mathrm{cm}^{-3}$) and finally a 220nm N^+-GaN contact layer (Si, $5 \times 10^{18} \mathrm{cm}^{-3}$). A two-step etching process was used to form the gate and drain trenches, whereby the gate trench was extended down to the N^+ drain layer during the second etching process [4]. To remove etch damage to the gate trench sidewalls, a 25% tetramethylammonium hydroxide (TMAH) treatment was performed at 80°C for 1 hour. Immediately following this, a 100nm SiO2 gate dielectric was deposited via PECVD. A SEM cross-section of the fabricated device is shown in Fig 1. Devices consisted of 3 gate trenches or unit cells, with a drain contact encircling the device mesa.

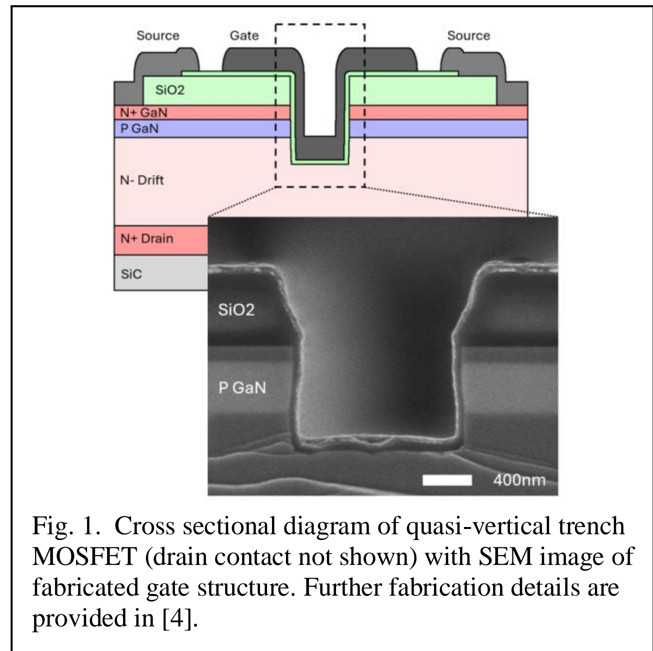

Fig. 1. Cross sectional diagram of quasi-vertical trench MOSFET (drain contact not shown) with SEM image of fabricated gate structure. Further fabrication details are provided in [4].

The fabricated devices were tested on a hot chuck probe station at temperatures from 25°C up to 150°C at a gate-drain voltage (V_{ds}) of 1 V. Devices were exposed to 365 nm UV illumination for 1 min immediately prior to temperature-dependent measurements to improve consistency. The UV treatment likely mitigates trapped charge effects at the MOS interface and within the floating p-body region [2, 3]. Without UV exposure, devices were found to exhibit a shift to higher threshold voltage under repeated measurements, which has previously been attributed to electron trapping at or close to the GaN/oxide interface [2, 3, 5, 6].

RESULTS

Temperature dependent transfer characteristics obtained for gate voltages in the range 0 V – 15 V are shown in Fig. 2, with the subthreshold region shown inset. An initial decrease in V_{th} is seen when temperatures are increased from 25°C to 75°C, followed by an increase in threshold voltage at higher temperatures. This non-monotonic threshold shift is suggestive of multiple temperature-dependent mechanisms responsible for the significant shifts in V_{th}. This instability is initially attributed to charge trapping/detrapping at the semiconductor-oxide interface and/or within the gate dielectric [2, 3, 5, 6]. Fig. 3 shows the quasi on-resistance (I_d/V_{ds} taken at the point of maximum transconductance g_m) normalized to active area, which follows a similar trend to V_{th}, suggestive of detrapping of negative charges leading to an earlier onset of inversion and increased conduction in the channel. Transconductance is also shown in Fig. 3, with faster turn-on as temperatures are increased above RT, indicating a lower density of interface states at the semiconductor-dielectric interface with increasing temperature. This trend is evident in the transfer curves shown in Fig. 2. The subthreshold slope (SS) was extracted from the points inside the shaded region inset in Fig. 2 (75°C and 100°C were excluded due to large negative shifts in V_{th}), which generally show a reduction from between 874 mV/dec at 25°C to 379 mV/dec at 150°C. These shallow subthreshold regions indicate slow turn-on due to e.g. capacitive trap filling. Although SS is related to interface trap density (D_{it}), extraction of D_{it} is complicated by the fact that SS is also a function of depletion capacitance, which is itself a function of temperature and p-body doping concentration. It is well known that acceptor ionization in GaN is typically much less than 10% for heavily doped Mg layers (activation energy of 220 meV) [7]. An increase in the fraction of ionized dopants with increasing temperature may also contribute to the positive shift in V_{th} seen at 125°C. Gate current I_g was found to remain below 0.1 nA across the temperature range, indicating good gate dielectric insulation and confirming

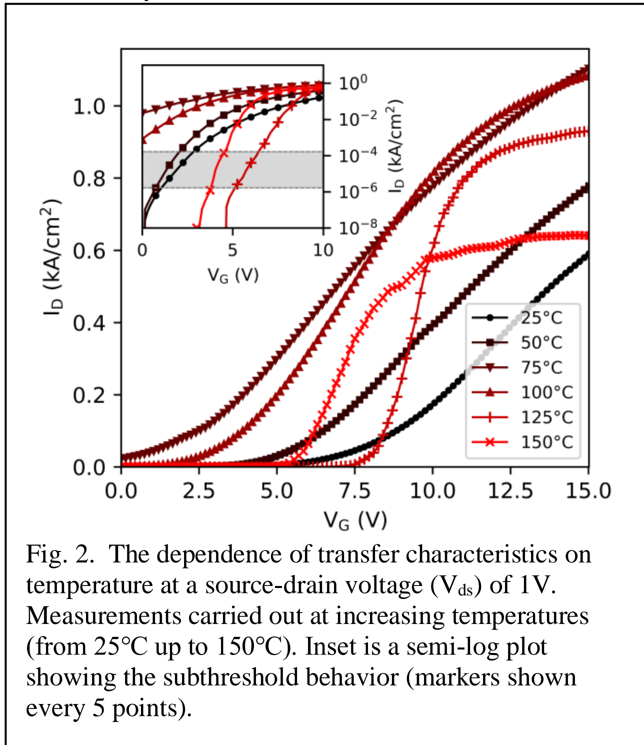

Fig. 2. The dependence of transfer characteristics on temperature at a source-drain voltage (V_{ds}) of 1V. Measurements carried out at increasing temperatures (from 25°C up to 150°C). Inset is a semi-log plot showing the subthreshold behavior (markers shown every 5 points).

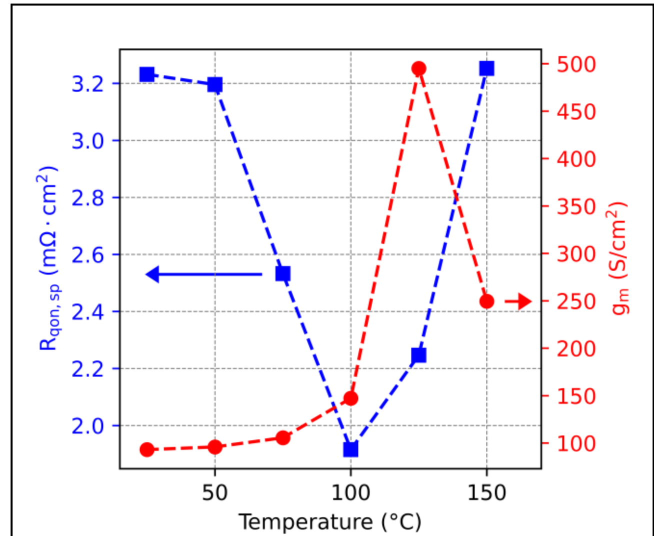

Fig. 3. Specific quasi-on-resistance and trans-conductance (both extracted at the point of maximum dI_d/dV_{gs}) shown as a function of temperature.

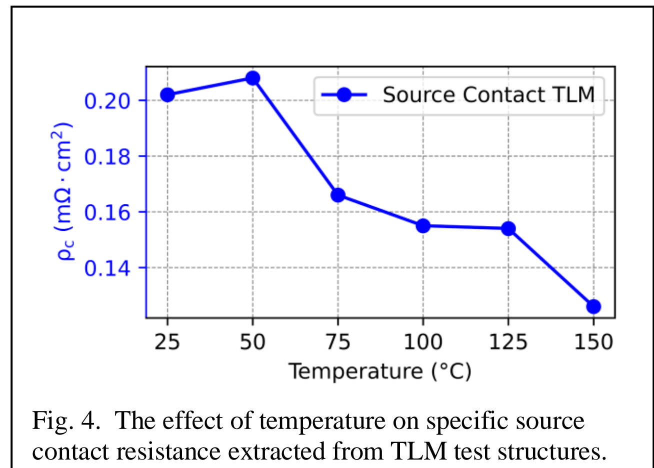

Fig. 4. The effect of temperature on specific source contact resistance extracted from TLM test structures.

negligible influence on the subthreshold current characteristics.

Series resistance contributions were subsequently investigated as a function of temperature using 4-point TLM measurements [8]. The specific contact resistance ρ_c of the source contacts was extracted using dedicated TLM test structures and is summarized in Fig. 4. Contacts were shown to exhibit a negative temperature co-efficient, with a decrease in ρ_c of 38% at 150°C compared with measurements taken at 25°C. Calculated resistance contributions from the source contacts were found to be negligible to the total R_{on} (~2%), even at lower temperatures. Similarly, drain contact resistance contributions can also be ignored due to the much larger area of the drain contact region compared with the source. The drain access region has been shown to introduce series resistance in quasi-vertical devices [9, 10], but is also ignored here due to the small number of gate trenches in the device and the proximity of the drain contact to the mesa edge. The encircling drain contact around the device mesa allows for current spreading in the drain region, helping to mitigate access resistance.

From the schematic in Fig. 1, in addition to the channel, the major series contributions to the total R_{on} are lateral access resistance through the N+ GaN source access region and contributions from the drift layer. It is useful to understand how these components contribute to conduction losses as a function of temperature, particularly over the typical operating range of the device. Estimates for both can be calculated from geometry once the GaN resistivity is known. Following Baliga, the source access resistance is treated trivially, while 45° current spreading in the drift layer is assumed [11].

The resistivity of both regions can be calculated using simple analytical approximations for the mobility and carrier concentration, which both depend on the doping concentration and temperature:

$$\rho = \frac{1}{q\, n(N_d, T)\, \mu_n(N_d, T)} \tag{1}$$

Dopant ionization dependance as a function of donor concentration and temperature was used to calculate electron concentration [7]. The semi-empirical model derived by Mnatsakanov et al. was then used to calculate the temperature and concentration dependencies on mobility [12].

The resistance values based on these calculations are shown in Fig. 5, normalized to the total on-state resistance at 25°C. Remaining resistance contributions are then attributed to the channel, although this includes small contributions from contacts and drain region, as indicated above. Although a large degree of uncertainty exists in the magnitude of these components, a strong dependence is not indicated across the temperature range. For the lowly doped drift layer where full dopant ionization is expected [7], a monotonic resistance increase indicates mobility degradation due to phonon scattering [11]. A small increase in resistance is also seen in the source access region, with mobility degradation countered by increased donor ionization at the higher doping

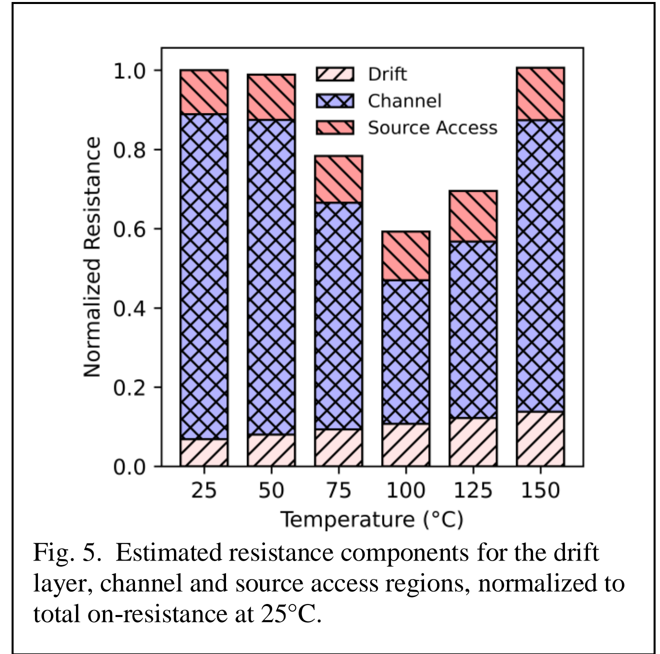

Fig. 5. Estimated resistance components for the drift layer, channel and source access regions, normalized to total on-resistance at 25°C.

concertation. This indicates that the channel contributions are dominant in determining the temperature dependent behavior of the MOSFET.

Conclusions

The on-state performance of quasi-vertical GaN MOSFETs on SiC was studied, revealing variability in threshold voltage, transconductance and on-resistance with increasing temperature. A maximum g_m of ~500 S/cm^2 was measured at 125°C, indicating improved gate control up to this temperature. Series resistance analysis demonstrates increased bulk GaN resistance contributions with increasing temperature from the N+ source access regions and the drift layer are predicted, with contacts contributing negligibly to total R_{on}. The channel is expected to dominate the on-state resistance, with trapping behavior at or close to the MOS interface likely responsible for the significant shifts in both threshold voltage and transconductance. Slow turn-on in the subthreshold region also indicates mitigation of interface traps is required to improve performance. These insights guide improvements for vertical GaN devices operating at higher temperatures.

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ACRONYMS

GaN: Gallium Nitride
SiC: Silicon Carbide
MOS: Metal-Oxide-Semiconductor
FET: Field Effect Transistor
HEMT: High electron mobility transistor
MOCVD: Metal-Organic Chemical Vapor Deposition
TMAH: Tetramethylammonium Hydroxide
PECVD: Plasma enhanced chemical vapour deposition
UV: Ultraviolet
SS: Subthreshold Slope
TLM: Transfer Length Method