Packaging of Compound Semiconductors – Current Status and Future Challenges

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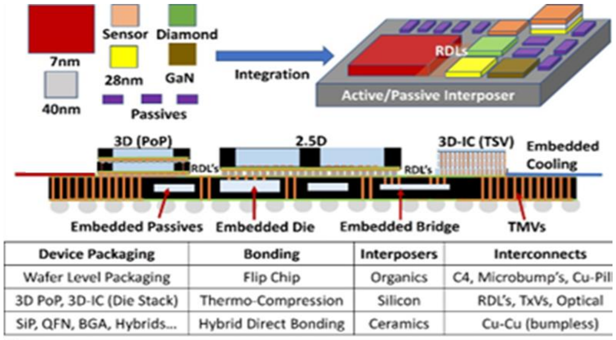
Keywords: Heterogeneous Integration, Modelling, Reliability

Abstract

Traditional packaging technologies such as wire-bonding and lead-frames have served the compound semiconductor market well. As industry moves towards heterogeneous integration, there is an evolving need for advanced semiconductor packaging technologies for compound semiconductors. Extending these technologies towards the compound semiconductor market faces several challenges in terms of wafer sizes, packaging materials, thermal management, and reliability. This paper discusses advanced semiconductor packaging technologies, the heterogeneous integration roadmap, and the need for modelling technologies to support the packaging of compound semiconductors, their performance and reliability.

INTRODUCTION

Compound semiconductors are used in a wide range of applications such as RF, sensing, power, and photonics. For micro-electronics and AI/HPC applications, Gordon Moore's seminal paper – Cramming More Components onto Integrated Circuits – published in 1965 [1] foresaw the limitations of transistor scaling and cramming as many of these onto a single chip. In this paper he stated "it may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected". Hence, in Moore's paper this statement essentially predicted the need for heterogeneous integration (HI) and advanced packaging, which is the cornerstone of today's chiplet technology



Device Packaging	Bonding	Interposers	Interconnects
Wafer Level Packaging	Flip Chip	Organics	C4, Microbump's, Cu-Pil
3D PoP, 3D-IC (Die Stack)	Thermo-Compression	Silicon	RDL's, TxVs, Optical
SiP, QFN, BGA, Hybrids...	Hybrid Direct Bonding	Ceramics	Cu-Cu (bumpless)

Fig. 1. Advanced semiconductor packaging toolbox for heterogeneous integration

Even though chiplets and advanced packaging provide faster times to market, improved yield, and use of appropriate technology node for the required function, they also face challenges. Challenges include complex interconnect designs within the package, thermal management solutions, as well as chip-package interactions (CPI).

ADVANCED SEMICONDUCTOR PACKAGING

The key roles of packaging – provide electrical connections, power connections, paths for thermal cooling, and protection – can be accommodated with traditional packaging technologies. For example, wirebonded and lead-frame based packages (e.g. QFP, QFN, etc) have served the community well and will continue to provide a good packaging foundation for many applications.

Fig. 1 illustrates the options and technologies for advanced packaging. Such technologies include interposers (or embedded bridges) and 3D stacking of chiplets using micro-bumps or hybrid bonding providing options for both 2.5D and 3D integration.

For HI applications, a combination of both 2.5D and 3D packaging technologies is attractive for cost-effective high bandwidth and low latency performance. Fan out wafer level packaging (FOWLP) is an ideal platform for heterogeneous integration where a diverse range of chiplets at different technology nodes, possibly with different semiconductor materials and functions, can be integrated and packaged on a reconstituted wafer.

FOWLP involves known-good-die being placed onto a carrier wafer. These dies are then over molded and then redistribution layers (RDL) are built-up to provide very fine line-spacing and high-density interconnection between dies and the outside world. FOWLP can be either die-first or die-last [2]. An example of FOWLP is the DECA M-Series Gen2 platform with adaptive patterning for routing between dies. This happens through automated optical inspection and real-time integration with EDA tools for pathfinding and design rule checks. This technology can achieve 20 µm bond-pad pitch, 2 µm L/S, and 2518 I/O/mm2 [3].

HETEROGENEOUS INTEGRATION ROADMAP

Heterogeneous integration of separately manufactured chiplets with different functions compliments homogeneous integration (e.g. system on chip – SoC) by enabling a systems approach to optimize system-level performance for applications such as AI/HPC, mobile devices, autonomous vehicles, medical devices, aerospace, and others. The 24 chapters of the HIR [4] provides a wealth of information on current state-of-the-art as well as a roadmap for future developments in advanced packaging including supporting technologies such as modelling and reliability.

CO-DESIGN & MODELLING

Predicting performance metrics such as signal/power integrity, thermals, and thermo-mechanical induced stress has been undertaken using high-fidelity tools such as ANSYS, Flotherm, Abaqus, Comsol, etc. A co-design approach (chip-package-system) is required to fully optimize package design in terms of system performance (electrical and thermal) and reliability (thermal and mechanical). Together with a multi-objective capability, these modelling tools provide a route to explore the chip-package-board design space and to ensure that performance and reliability metrics are met, and the risk of failures are mitigated.

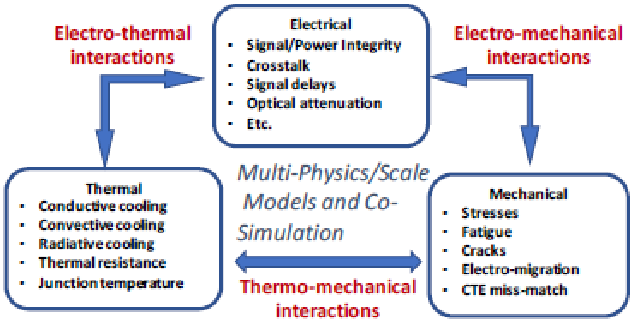


Fig. 2. Interaction between physical domains

Fig. 2 illustrates the key physical phenomena that needs to be predicted in the electrical, thermal and mechanical domains. Mapping power distributions from a chip model to temperature distributions at the package and system levels is an example of interactions at the electro-thermal interface.

For the thermo-mechanical interface, examples include accurately leveraging the thermal stress resulting from a package/system model into the backend of the chip to predict physical stress and damage in the regions of the through-silicon vias (TSVs). These stresses will impact the layout of the TSVs as well as the transistor threshold voltages and drive currents. A classic example of electro-mechanical modelling is electro, thermal and stress-migration in interconnects both on and off the chip. These are only a small list of examples that demonstrate the need for co-design and multi-physics analysis across the chip-package-system domains, and the need to accurately model the interactions between electrical, thermal and mechanical domains.

RELIABILITY

Compound Semiconductor chips and passive electrical components are vulnerable to both global and local sources of stress, where global stresses result from co-efficient of thermal expansion (CTE) and co-efficient of moisture expansion (CME) mismatch between the chip, package, and board materials, and local stresses arise from temperature gradients due to self-heating effects within the chip. At the chip level, these stresses can result in die cracking, under-bump metallization (UBM) cracking/delamination, back-end-of-line (BEOL) failures, through-silicon-via (TSV) delamination/cracking, metal migration and voiding, and mobility shifts in transistor performance.

Fig. 3 details an example of a test flow for qualifying semiconductor packages (component-level tests). A statistically significant number of components are subjected to environmental stresses in each test. Components for both thermal cycling and HAST are first subjected to preconditioning to capture the residual stresses they would see during a solder reflow process. The same number of components are also subjected to the high temperature storage test without preconditioning as this test assesses the impact of component storage environments with regards allowed moisture uptake.

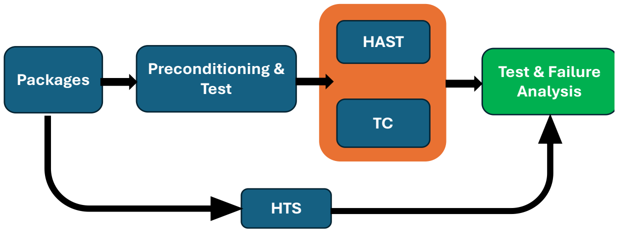


Fig. 3. Package-Level Reliability Test Flow

Fig. 4 details a test flow for board-level reliability. Again a statistically significant number of boards will be subjected to environmental stress conditions such as thermal cycling (for example, investigating the thermo-mechanically induced fatigue behavior of second level interconnects between the package and PCB) as well the drop test where PCB's are subjected to mechanical shock to assess the robustness of second-level interconnects and fixtures to repeated drops (typically 200).

Industry follows standards such as JEDEC to test for failure modes and mechanisms. These tests accelerate in time the expected failure mechanisms through subjecting the packages to temperature, moisture, electrical, and mechanical loads.

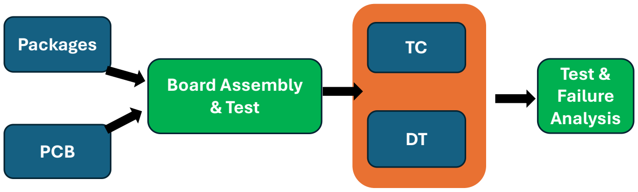


Fig. 4. Board-Level Reliability Test Flow

Table I details the type of JEDEC tests that would be undertaken in the above test flows.

TABLE I

STRESS TESTS FOR RELIABLITY ASSESSMENTS

Stress Test	**Typical Conditions**	**Used for:**
Pre-conditioning	Moisture Sensitivity Levels	Simulation of shipment and moisture impact to solder reflow.
Thermal Cycling (TC)	-55/125C, 700 to 850 cycles	Fatigue life
High Temperature Storage (HTS)	125C or 150C for 1000 hours	Oxidation, degradation of organics, inter-metallics
HAST	130C/85%RH for 96 hours	Corrosion, delamination, metal-migration
Drop Test (DT)	Various Specs	Strength of attachments, mechanical fixturing.

MODELLING EXAMPLES

Packaging processes such as building RDL, molding, and bonding can induce stresses and failures that will impact overall quality of the packaged assembly and hence subsequent reliability. These processes are highly non-linear where high-fidelity simulations require accurate process dependent material properties such as viscoelastic flow properties for simulating a molding process. Hence the strong link between metrology and modelling is required to ensure accurate model predictions.

An example of process modelling of packaging processes includes predictions of warpage that occur during the fan-out-wafer-level packaging (FOWLP) process steps as shown in Fig. 5. Ensuring that warpage is controlled is a major requirement for FOWLP as the consequences for high warpage impacts subsequent process conditions and overall reliability of the package due to chip-cracking, bonds detaching, and RDL delaminating.

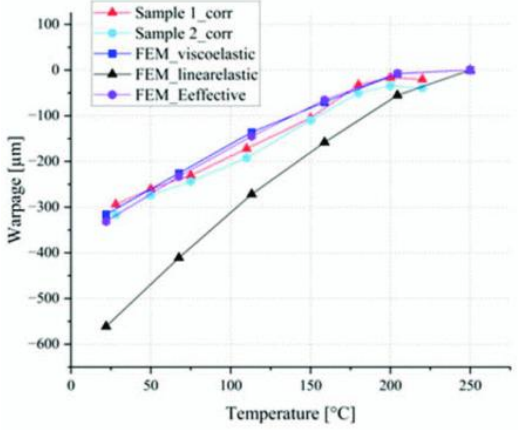


Fig. 5. Modelling Warpage in FOWLP process: comparison between linear and non-linear models [5]

Another key process that can impact package quality and hence reliability is the interconnect bonding process such as flip-chip bonding for die-to-die stacking. A key requirement here is to understand the impact of alignment accuracy on the quality of the fabricated bonds for high interconnect applications. Techniques such as solder micro-bumps formed during a reflow process, thermo-compression bonding, and copper-copper hybrid bonding can be used depending on the bump pitch required.

An example of numerical modelling of the flip-chip bonding process has investigated thermo-compression bonding of indium bumps for focal plane arrays where a compound semiconductor pixel array IC is bonded to a silicon read-out IC die [5]. As detailed in Fig. 6, the impact of misalignment can have serious consequences on bond quality where larger misalignment leads to bump collapse and very small stand-off heights for the formed bonds. This will lead to very poor subsequent reliability due to CTE mismatch in the materials. This work demonstrated that for ultra-fine pitch applications an alignment accuracy of sub-um was required to avoid bump collapse.

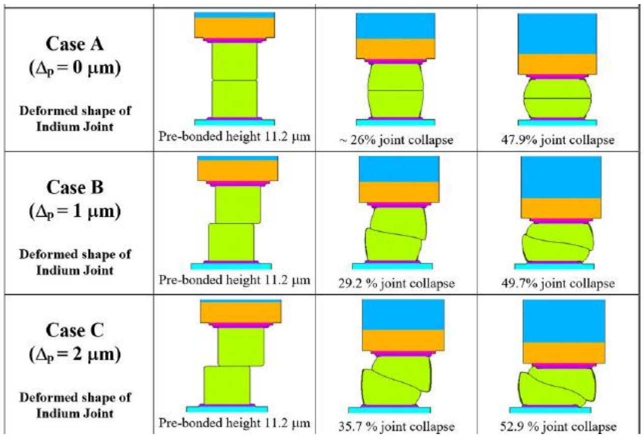


Fig. 6. Modelling thermo-compression bonding process for die-die stacking focal plan array application [6]

After a package is fabricated, it will undergo component level and board level qualification as per the JEDEC specifications. These tests expose the package and board to thermal, vibration, and humidity induced stresses. Using modelling to virtually assess a package's thermo-mechanical performance before physical prototyping can result in extensive cost savings as well as ensure a package design and architecture meets the required reliability specifications.

Fig. 7 details an example of a solder bump model at the package-PCB interface. In this analysis, the design of the PCB and the use of additional materiasl such as underfills and edgebonds were investigated to minimize the risk of early fatigue damage to these interconnect structures. Simulation results show that the highest plastic work (an indicator for crack initiation and fatigue failure) occurs at the solder bump/PCB interface for this design.

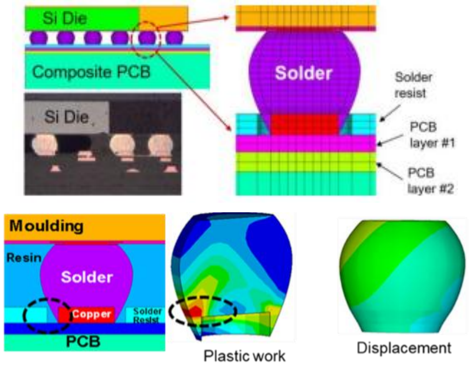


Fig. 7. Solder interconnect models and predictions of plastic work when subjected to a thermal load [7]

Fig. 8 details model predictions for different PCB's and clearly identifies the impact of both edgebonds and underfills as options to stress relieve the solder joints when subjected to thermal loads and hence minimizes the risk of early fatigue failure.

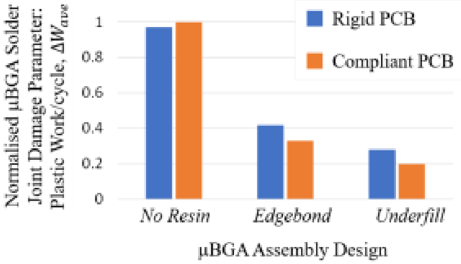


Fig. 8. Model predictions of damage in the solder interconnects and impact of different material choices [7]

FUTURE CHALLENGES

To support developments in advanced packaging for heterogeneous integration of compound semiconductors, challenges in new packaging materials and thermal management need to be addressed. Modelling developments are also required to ensure performance and reliability metrics are met early in the design processes. Fig. 9 illustrates this evolving capability. A hierarchy of modelling techniques: (1) high-fidelity multi-physics/scale models (e.g. FEM, Molecular Dynamics, etc) (2) reduced-order-models (e.g. physics-informed neural-networks, etc) and (3) digital twins are required to support chip-package-system co-design and to ensure that package performance and reliability specifications are met at the early stages of package design. To support this, metrology techniques are required to ensure that accurate model input data is available. For example, we can envisage a future where each piece of equipment in a packaging process flow includes a digital twin to ensure optimal manufactured quality. Such physics-informed digital twins can also be used in ALT's to identify if and when packages will fail early in the test cycle saving significantly on cost of these tests.

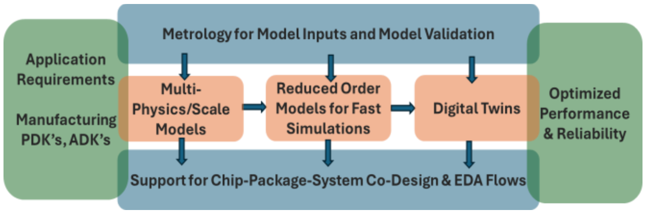


Fig. 9. Modelling & simulation requirements to support package performance, reliability, and co-design.

CONCLUSIONS

Compound semiconductor chiplets for applications such as power, photonics, communications, sensing and processing will require advanced semiconductor packaging technologies to meet their goals in heterogeneous systems. This paper has detailed trends in advanced semiconductor packaging (e.g. FOWLP, 2.5D, and 3D, etc). Techniques for modelling and reliability will play a key role as we move towards heterogeneous systems.

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ACRONYMS

ALT: Accelerated life tests
CTE: Co-efficient of thermal expansion
FOWLP: Fan out wafer level packaging
HIR: Heterogeneous Integration Roadmap
HI: Heterogeneous Integration
PCB: Printed circuit board
RDL: Redistribution layers
TSV: Through silicon via