Heterogeneous Integration of Large-Area InGaAs SWIR Photodetectors on 300 mm CMOS-Compatible Si Substrates

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Abstract

We demonstrate the heterogeneous integration of SWIR large-area InGaAs photodetectors and pixelated photodetector arrays on 300 mm CMOS-compatible Si (100) substrates through direct heteroepitaxy. The devices exhibit low dark current, high responsivity, low capacitance, and high quantum efficiency at shortwave infrared wavelengths.

Introduction

High-performance, scalable, and cost-effective sensors are essential for applications in autonomous systems, robotics, aerospace, quantum information, artificial intelligence, mobile devices, and AR/VR. While silicon (Si) complementary metal-oxide-semiconductor (CMOS) sensors dominate visible and near-infrared detection (up to ~940 nm), they lack capability in the shortwave infrared (SWIR) spectrum (900–1700 nm) where demand is growing for consumer, defense, and aerospace markets. SWIR offers distinct advantages, including reduced solar interference for reliable outdoor performance, and compatibility with established SWIR components, such as lasers, all of which are critical for 3D imaging in autonomous systems. Furthermore, SWIR enables night vision and imaging in challenging weather conditions, while supporting eye-safe operation. These attributes support enhanced resolution and range for facial recognition, light detection and ranging (LiDAR), and other 3D imaging applications.

Incumbent Si detectors are highly scalable and mature, but their efficiency degrades beyond 940 nm, limiting their utility in SWIR bands. Traditional SWIR detectors, such as InGaAs-on-InP, provide high efficiency but remain costly and limited in scalability due to fragile, small-diameter substrates. Emerging alternatives such as Ge-on-Si and colloidal quantum dots (CQDs) offer scalable pathways but have yet to demonstrate proven performance in key SWIR bands [1]. To address these limitations, Aeluma has developed a direct heteroepitaxy approach for InGaAs-on-Si to realize scalable, high-performance SWIR sensors, leveraging large wafer sizes to enable large-scale production and wafer-scale integration.

Scalable Direct Heteroepitaxy of III-V Semiconductors on Silicon

Aeluma leverages metalorganic chemical vapor deposition (MOCVD) for the synthesis of InGaAs-based detector structures on large-diameter substrates [2]. The detector material is deposited on an optimized III-V buffer grown on up to 12-inch Si (100), as illustrated in Fig. 1(a). A combination of dislocation filtering approaches was implemented, using methodologies similar to those described in Ref. [3, 4], to achieve a low dislocation density. A surface roughness as low as 1.74 nm was achieved for a 10 µm×10 µm AFM scan. It should be pointed out that for the InGaAs absorber grown on III-V-on-Si templates, a separate InGaAs growth calibration is needed to compensate the composition shift due to the residual strain in the buffer as well as the slight deviation of surface temperature (different thermal conductivity and emissivity) for III-V-on-Si substrates, as compared to the growth of photodetector on native III-V substrates.

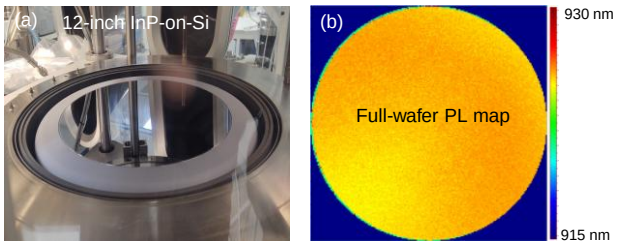

Fig. 1. (a) Direct epitaxy of 300 mm InP buffer on CMOS-compatible (001) Si substrates, and (b) room-temperature photoluminescence (RT-PL) mapping of the InP buffer.

High-Performance and Scalable InGaAs SWIR Photodetector Manufacturing

Large-area photodetectors of various sizes and geometries were fabricated as illustrated in Fig. 2. The fabrication process includes p-contact metallization, mesa etching, passivation, n-contact via opening, and n-contact metallization. During the fabrication, we did notice a slight difference in the etching rate and passivation processes for the photodetectors grown on native III-V substrates and on Si, due to slightly different

effective surface temperatures and higher roughness on Si. Fortunately, the deviation is minimal, and this can be addressed by optimizing the lithography process and tailoring plasma etching time for photodetectors on Si. The chemicals and treatments applied to both photodetectors grown on native and on Si substrates are identical. Additionally, we did not observe an apparent impact of wafer bowing on the manufacturing process and device yield, attributed to the thick Si substrates and the control of the total III-V buffer thickness.

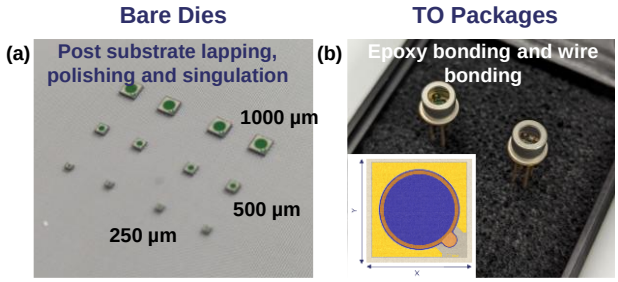

Fig. 2. (a) Post processing of devices and singulation into bare dies; (b) Detectors integrated in TO packages. Inset shows the layout of a single large-area photodetector.

The fabricated wafers undergo screening with wafer-level semi-automatic dark current characterization, followed by substrate lapping into approximately 200 µm thickness, backside substrate polishing, and dicing or cleaving into bare dies (Fig. 2(a)). Thinned photodetector chips are firstly epoxy bonded to AlN submounts. These subassemblies were subsequently epoxied onto the TO header and wire-bonded to create electrical connections to the TO pins. Finally, the TO lid is welded to the TO header (Fig. 2(b)). The device package into TO cans facilitates additional detector characterizations, including optical response measurements and aging test.

InGaAs-on-Si Photodetector Characterization

The electrical and optical characteristics of the 1310 nm InGaAs large-area photodetector grown on Si are presented in Fig. 3. The uncooled devices demonstrate a dark current density as low as 8.47 µA/cm² at room temperature (25°C) under a reverse bias of -5 V. To our knowledge, this represents the lowest dark current density reported for SWIR photodetectors grown on Si, attributed to superior material crystalline quality and proprietary epitaxial structure design.

To analyze the dark current contributors, measurements were conducted on photodetectors of varying diameters (D), as shown in the inset of Fig. 3(a). The total dark current density can be expressed as $J_d = J_{bulk} + 4 \cdot J_{surf}/D$, where J_{bulk} and J_{surf} represent bulk and surface leakage, respectively [5]. This analysis indicates that surface leakage introduced during device fabrication constitutes a primary source of dark current in these large-area InGaAs photodetectors on Si. Figure 3(b) demonstrates optical response of InGaAs photodetectors characterized using an external 1310 nm laser, a wavelength of particular interest for mobile devices, automotive 3D imaging, and industrial applications. A cleaved single mode fiber was used to couple 1310 nm laser through the top of the device mesa vertically. The QE extrapolated in the inset of Fig. 3(b) reaches approximately 53% (measured R=0.56 A/W) at 1310 nm, with potential for improvement through increased absorption layer thickness. As a reference, the QE of detectors on III-V native substrates with identical dimensions were measured at 61% (measured R=0.65 A/W). The comparable optical response validates the competitive performance of the InGaAs-on-Si photodetector. The InGaAs-on-Si device capacitance was also measured as shown in Fig. 3(c). The low terminal capacitance is comparable to commercial InGaAs photodetectors with similar device dimensions, enabling high-speed operation. It should be noted that the absorption

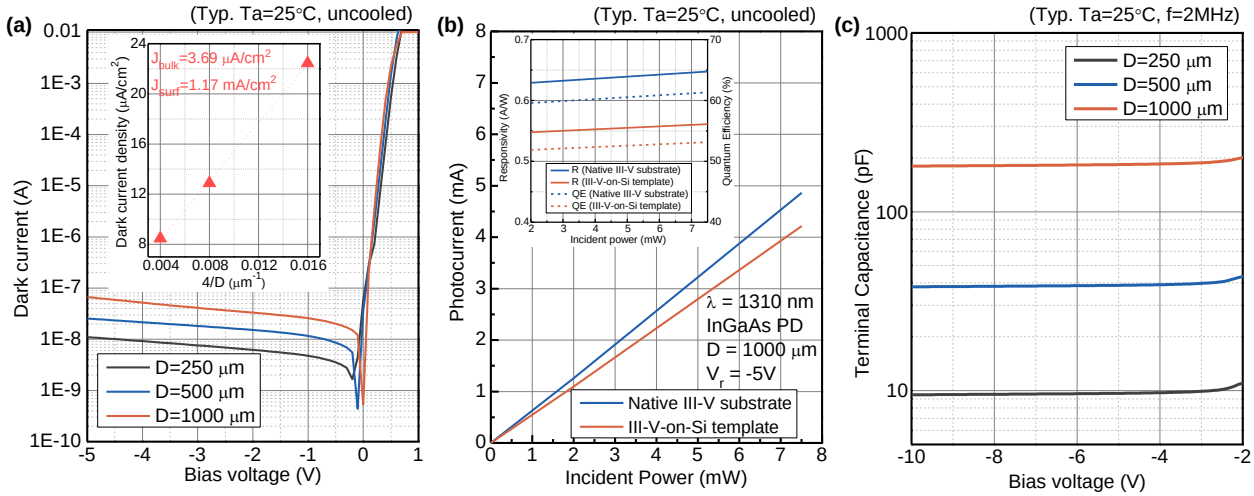

Fig. 3. Electrical and optical characterization of InGaAs-on-Si photodetectors: (a) Dark current versus reverse bias voltage for varying device dimensions, with inset showing extracted dark current density as a function of device diameter; (b) Optical response curves for detectors on III-V and Si substrates, with inset showing the optical responsivity (R) in solid lines and quantum efficiency (QE) in dashed lines; (c) Capacitance-voltage characteristics for photodetectors of different dimensions.

layer thickness design necessitates careful optimization to balance the inherent trade-off between quantum efficiency and speed, where the latter is constrained by both capacitance and carrier transit time.

epitaxial layer structures, the updated "SPDA-L" series achieve considerably lower dark currents for high-temperature operating environments such as LiDAR for autonomous vehicles. The dark current at 105°C reduced from 18 nA (SPDA-M) to 2.4 nA (SPDA-L), as shown in Fig. 4(e).

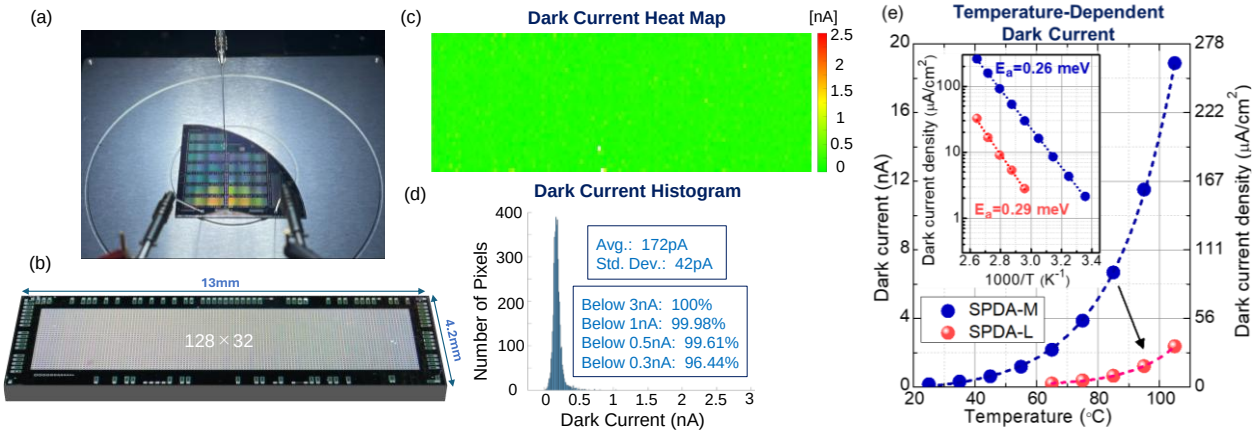

Fig. 4. (a) Photograph of a fabricated PDA on Si quarter wafer. (b) Exemplary singulated 128×32 PDA chip with a pixel pitch of 90 μm. (c) Dark current heat map of the 128×32 SPDA-M series at room-temperature. (d) Extrapolated histogram for yield analysis. (e) Dark current of a single detector pixel as a dependence of the stage temperature for both SPDA-M and-L series. Inset shows the extrapolation of the activation energies for the two PDA structures. The operating bias is -5 V for all the measurements.

InGaAs-on-Si Photodetector Arrays and Integration Pathway

To expand the portfolio of our products and enable hyperspectral imaging for spectrometer applications with larger dynamic range and background rejection, we also developed highly pixelated photodetector arrays (PDAs), as demonstrated in Fig. 4. Figure 4(a) provides an image of SWIR PDA wafer manufactured with Aeluma's platform. Our customized format varies from 128×32 to 640×512 pixels, commonly used for video graphics array (VGA) cameras. Pixel sizes and pitches also vary from a few μm to tens of μm, and Fig. 4(b) displays an exemplary singulated 128×32 PDA chip ("SPDA-M" series) with 85×85 μm^2 active area pixels (pitch of 90 μm). The dark current heat map and the histogram of the PDA are presented in Figs. 4(c) and 4(d), demonstrating an excellent uniformity, high yield, and state-of-the-art average dark current as low as 172 pA under a reverse bias voltage of -5V at room temperature [6]. By engineering the

The dark currents for SPDA-L are even lower than the measurement limit between RT and 60°C. Here, the dark current reduction is primarily attributed to a larger activation energy (E_a) for SPDA-L series, as shown in the inset of Fig. 4(e).

Aeluma's large-diameter InGaAs-on-Si photodetector wafer allows for a new paradigm of advanced packaging for the 300 mm wafer-scale heterogeneous integration of PDAs on CMOS readout integrated circuit (ROIC) wafer through wafer-to-wafer (W2W) hybrid Cu-Cu bonding. Figure 5 illustrates the target integration process, including the post processing steps such as substrate lapping, polishing, metallization, and coating etc. An ultra-high integration density along with larger pixel formats and the shrinkage of PDA pixel size can therefore be enabled, which would be revolutionary for the SWIR imaging industry.

Conclusions

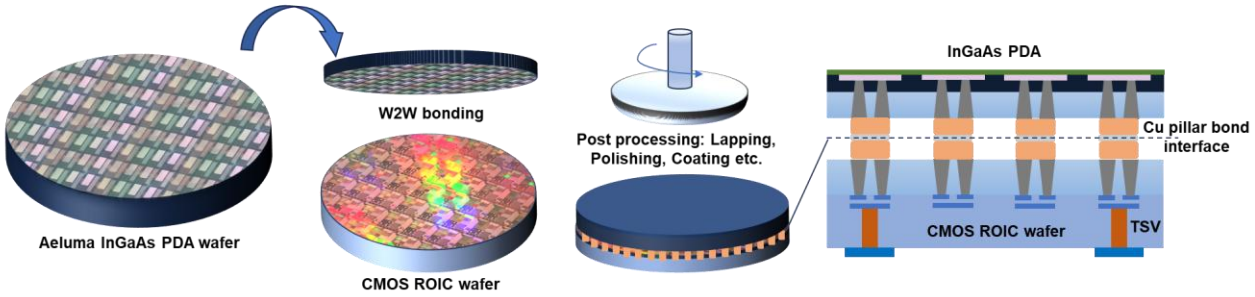

Fig. 5. Aeluma's large-diameter wafer InGaAs PDA platform is amenable to 300 mm wafer-scale integration, which enables performance enhancement, scaling and cost reduction.

We have successfully demonstrated the heteroepitaxy of high performance InGaAs SWIR photodetectors on a 300 mm Si substrate platform. The large-area detectors demonstrate record-low dark current density of 8.47 μA/cm² (-5V bias), a high quantum efficiency of 53% at 1310 wavelength band, and a low capacitance of 10 pF. Additionally, we manufactured ultralow dark current PDAs particularly suitable for high temperature operations. The PDAs exhibit a superior uniformity and high yield, revealing a dark current of 2.4 nA at 105°C environment temperature, biased at -5V. These results demonstrate the potential for producing low-cost, high-performance SWIR sensors utilizing large-scale Si manufacturing capabilities, further advancing photon detection capabilities and establishing a pathway for 300 mm wafer-scale heterogeneous integration with CMOS ROICs for a broad range of applications.

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ACRONYMS

SWIR: Shortwave Infrared
LiDAR: Light Detection and Ranging
InGaAs: Indium Gallium Arsenide
Si: Silicon
Ge: Germanium
CQD: Colloidal Quantum Dot
CMOS: Complementary Metal-Oxide-Semiconductor
AR/VR: Augmented Reality/Virtual Reality
InP: Indium Phosphide
TO: Transistor Outline
RT: Room Temperature
PL: Photoluminescence
R: Responsivity
QE: Quantum Efficiency
PDA: Photodetector Array
VGA: Video Graphics Array
ROIC: Readout Integrated Circuit
W2W: Wafer-to-Wafer
Cu: Copper
TSV: Through Silicon Via