Advanced Process Development for Microcavity VCSELs

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ABSTRACT

In this work, we report the development of a high-precision fabrication process for microcavity VCSELs operating at cryogenic temperatures with oxide-aperture sizes below 3 μm. To address the critical challenge of controlling oxide-aperture size during wet oxidation, a novel hybrid etch mask combining SiNx and PR was introduced, enabling vertical mesa sidewall profiles with improved reliability and process uniformity. This approach enhances the accuracy of oxide formation, crucial for scaling down VCSEL apertures while maintaining thermal and optical performance. The fabricated Cryo-VCSEL with 1.7 μm aperture demonstrates exceptional output power of 3.93 mW and modulation bandwidth exceeding 50 GHz at 2.9 K, with successful PAM-4 data transmission at 112 Gbps. The process yields minimal aperture variation (~ 0.5 μm IQR) across samples, ensuring suitability for parameter extraction and VCSEL array integration. These advancements establish a scalable fabrication platform for high-speed, cryogenic VCSELs, supporting future optical interconnects in quantum computing systems.

INTRODUCTION

The VCSEL has been widely adopted for high-speed data communication due to the discovery of AlGaAs oxidation by Dallesasse and Holonyak [1]. This innovation provided the critical lateral cavity confinement of photon and carrier in semiconductor lasers, which made the oxide-confined VCSEL to be low threshold (I_{TH} < 1 mA), low power operation, and become the practical solution for short-haul data transmission that has been widely used in data centers. Lately, researchers are now exploring the potential of oxide-confined VCSELs at cryogenic temperatures under high modulation bandwidth to meet the demands of data transmission in cryogenic computing [2, 3]. Unlike operation at RT, where oxide apertures (< 6 μm) can pose reliability challenges due to self-heat dissipation issues, cryogenic temperatures offer enhanced heat transfer, making it feasible to experiment with small oxide aperture designs.

In this study, we have developed microcavity VCSELs that operates at cryogenic temperatures (Cryo-VCSEL) featuring an oxide-aperture size (< 3 μm). This includes achieving a vertical sidewall profile for the controllability of the small oxide-aperture size during the wet oxidation process. In our research, we have successfully attained a vertical slope of the mesa sidewall, which plays a critical role in maintaining control during the wet oxidation process that generates the oxide aperture of under 3 μm. The microcavity VCSEL with aperture size ~ 1.7 μm achieves impressive laser output power of 3.93 mW with a bandwidth exceeding 50 GHz at cryogenic temperatures.

To create the oxide-aperture, the mesa must first be etched down with the sidewall exposed. Subsequently, it is placed in a wet furnace, allowing water vapor to diffuse into the mesa and interact with the AlGaAs layers to form AlOx from the surface of the mesa sidewall. Typically, the rate of oxide formation is uniform across the mesa structure and is highly influenced by the aluminum content in the AlGaAs layer. Consequently, the control of the oxide-aperture size is contingent upon the mesa size where the high aluminum content AlGaAs layer is situated, as well as the duration the sample remains in the wet furnace.

A non-vertical sidewall profile can lead to discrepancies between the designed mesa size and the actual mesa size containing the high aluminum content AlGaAs layer, resulting in diminished process controllability. Furthermore, our control over the oxidation rate is significantly dependent on top-view images captured by an IR camera [4]. In the absence of a near-vertical sidewall, defining the oxide-aperture boundary in the infrared image becomes increasingly difficult.

To mitigate this issue, we propose a hybrid etch mask that combines a SiNx hard mask with a PR resist mask for mesa dry etching, which provides excellent selectivity. This innovative approach facilitates the formation of a nearly vertical sidewall profile on VCSEL epitaxial wafers, thereby enhancing control and reliability throughout the process.

EXPERIMENTAL DETAILS

Our high-speed VCSEL fabrication process [5] begins with P-metal deposition, followed by mesa etching using Chlorine-based ICP-RIE, oxide aperture formation, and N-metal deposition. BCB is then spin-coated for planarization, serving as a dielectric for signal isolation. Finally, vias are

etched, and metal interconnects are deposited to form the signal waveguide.

Initially, we used PR as the etch mask for mesa dry etching, tested with a stripe pattern shown in Fig. 1. The cross-sectional SEM image of the dry-etch result, shows a slanted sidewall, indicating a highly isotropic etch profile with poor selectivity. Increasing RF power in ICP-RIE to achieve greater anisotropy further reduces selectivity between the mask and wafer, limiting this approach's effectiveness. Using a SiNx film as a hard mask with higher RF power can improve both selectivity and anisotropy, but the required thickness for adequate mesa etch depth causes stress issues. At the necessary thickness, SiNx is prone to fracture from film stress, making it unreliable.

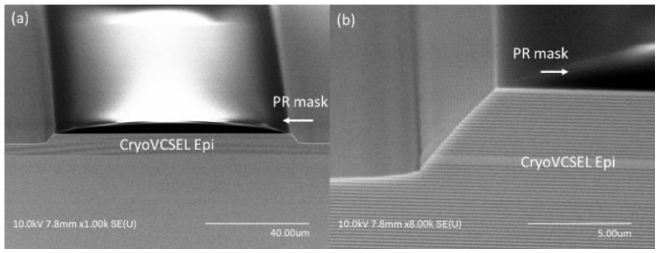

Fig 1. SEM cross-sectional view of the etch profile with PR mask. (b) is the enlarged view of (a).

To overcome these challenges, we developed a hybrid mask that combines the advantages of both PR and SiNx masks while minimizing their limitations. This hybrid mask consists of a thin 150 nm SiNx layer at the bottom, topped with a 5 µm PR layer. The fabrication process flow for this hybrid mask, shown in Fig. 2, involves depositing a thin SiNx film via PECVD, coating it with PR, and then performing lithography to define the mesa region. The SiNx is then etched using Freon-based ICP-RIE to transfer the mask pattern, allowing for final mesa etching with Chlorine-based ICP-RIE.

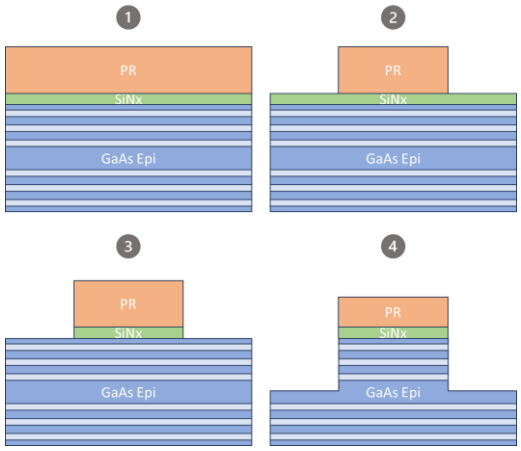

Fig 2. Hybrid etch mask fabrication process flow diagram.

Results and Discussion

The result of using this hybrid mask for mesa etching is shown in Fig. 3. Fig. 3 (a) demonstrates the etching outcome on a plain GaAs substrate, while Fig. 3 (b) shows the result on a Cryo-VCSEL epi wafer with DBR pairs. This technique achieves nearly identical vertical etching sidewall profiles for both wafer types, making the hybrid mask versatile across different substrates. In Fig. 3, the upper edge of the hybrid mask still shows signs of lateral etching, similar to Fig. 1. However, the lower part of the hybrid mask is more vertical compared to Fig. 1 due to the protection from thin SiNx film underneath. Adding just 150 nm of SiNx produces a noticeably different etching profile. The high selectivity of the SiNx mask prevents the PR mask from begin etched by the ICP-RIE, leaving much of the PR mask intact. The thickness of SiNx film can be significantly reduced compared to using SINx alone as an etch mask since the remaining PR mask now provides most of the blocking function. This reduced thickness eliminates the risk of film fracture due to stress.

The hybrid mask technique was effectively employed to complete the microcavity Cryo-VCSEL fabrication process, achieving oxide-aperture sizes of 1.7, 2.3, and 2.6 µm. The fabricated device is illustrated in Fig. 4, while Fig. 5 provides a detailed statistical analysis of the oxide-aperture sizes across various samples, highlighting the differences in target sizes and designed mesa diameters. The hybrid etch mask guarantees a vertical sidewall profile while also providing excellent uniformity across the same sample. The analysis depicted in Fig. 5 suggests that the IQE is approximately 0.5 µm, indicating a minimal degree of size variation. Ensuring process uniformity within a single sample is crucial, particularly for parameter extraction, device modeling, and VCSEL arrays. Consistent device performance across the sample is essential for accurate parameter extraction, which in turn instills confidence in the device model developed from the extracted parameters.

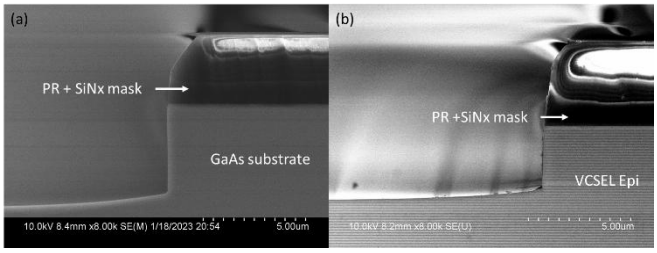

Fig. 3. SEM cross-sectional view of sidewall etch profile of using the hybrid etch mask. (a) Etch profile of plain GaAs substrate. (b) Etch profile of VCSEL epi wafer with DBR.

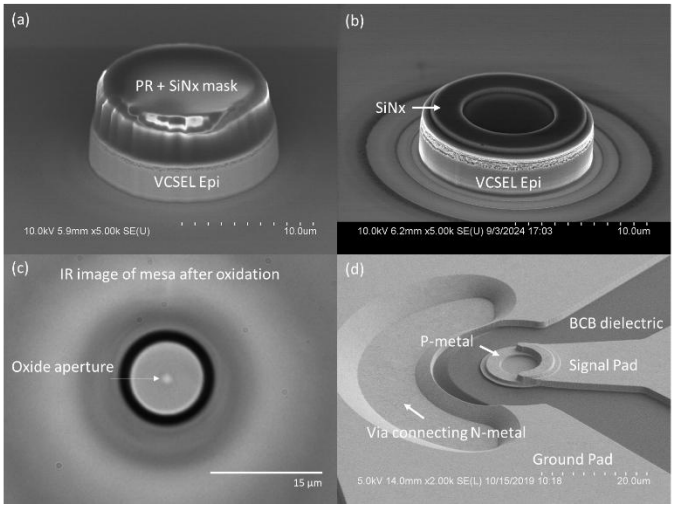

Fig. 4. Images of the Microcavity Cryo-VCSEL utilizing a hybrid etch mask during the fabrication process are presented. (a) SEM image of the mesa structure after etching. (b) SEM image of the mesa structure following the removal of the PR. (c) IR image of the oxide-aperture process monitor, demonstrating exceptional control over oxide-aperture size, achieving precision down to approximately 1 µm. (d) SEM image of the fabricated Microcavity.

The LIV curve measurements are presented in Fig. 6. The LIV curve shows the scaling effect of the oxide-aperture size on the thermal roll-over point and maximum output power that they both related to the self-heating from the shrinking aperture size. The microcavity Cryo-VCSEL, featuring an aperture size as small as 1.7 µm, demonstrates impressive laser output power of approximately 3.93 mW, accompanied by a bandwidth exceeding 50 GHz at cryogenic temperatures, making it suitable for high-speed data transmission. Further investigation on the oxide-aperture scaling effects detailed in our recently published research, which presents the first study on the scaling effects of cryogenic VCSELs, achieving record output power density [6].

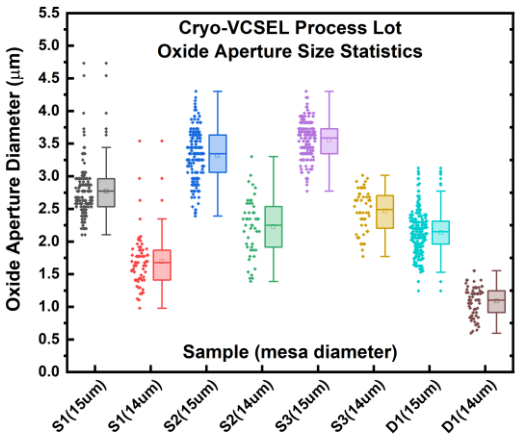

Fig. 5. Statistical analysis of oxide-aperture sizes across diverse samples, focusing on various target sizes and incorporating different mesa diameter designs. All samples underwent the same processing procedure except for the oxidation time in the wet furnace.

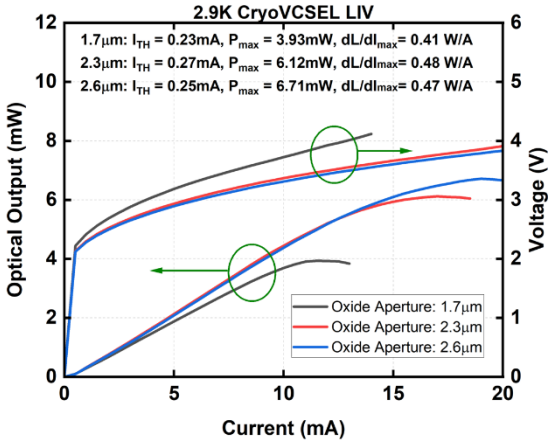

Fig. 6. LIV curve of microcavity Cryo-VCSEL with three different oxide-aperture size.

Fig. 7 presents a comparison of the laser spectra for Cryo-VCSELs operating at 2.9 K with oxide-aperture size of 1.75 µm and 6.80 µm under a bias current of 1 mA. Both devices exhibit identical threshold currents of 0.25 mA. The data indicates that the lasing modes of the 1.75 µm device are significantly fewer than those of the 6.80 µm device, suggesting that the optical mode volume is considerably reduced by the size of the oxide-aperture.

Fig. 8 demonstrates the 112 Gbps PAM-4 optical eye diagram for a Cryo-VCSEL operating at a bias current of 6 mA, with an oxide-aperture size of 2.68 µm at a temperature of 2.9 K. The eye diagram was processed using the standard TDECQ qualification integrated within the Keysight DCA-X N1000A. This analysis computes an effective power penalty following the application of a standard linear 4-tap FFE. The depicted clear eyes in the figure demonstrate a promising capability for high-speed performance at cryogenic temperatures, suggesting that microcavity VCSELs could be viable candidates for the next generation of optical high-speed data links.

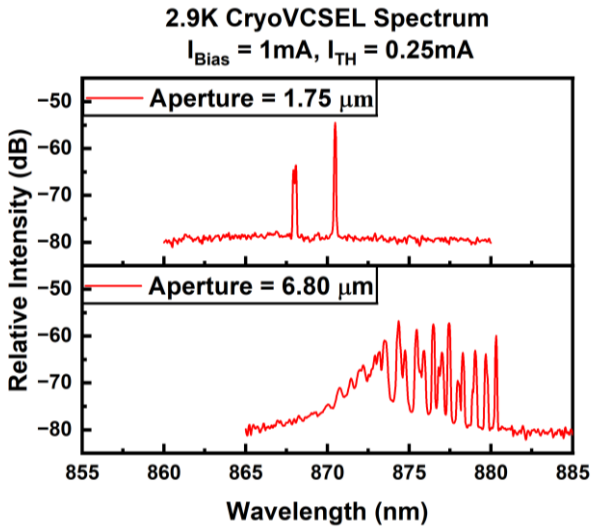

Fig. 7. Spectrum comparison of Cryo-VCSEL with different oxide-aperture size at 1 mA bias.

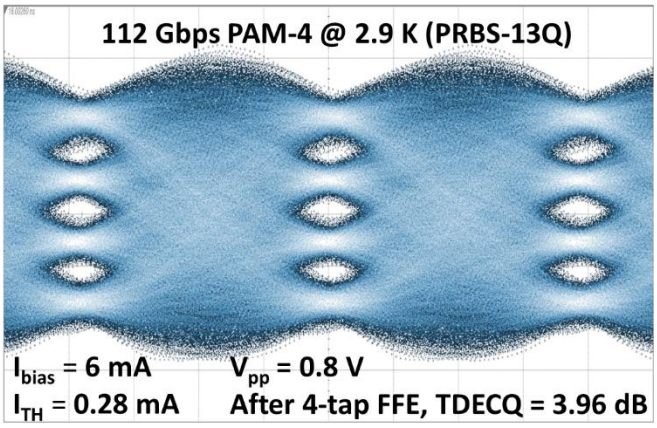

Fig. 8. Cryo-VCSEL 112Gbps PAM-4 optical eye diagram at 2.9 K with 2.68 μm oxide-aperture. The driven bias and driven RF amplitude are labeled within the figure.

Conclusions

To develop the fabrication process for microcavity Cryo-VCSELs with an oxide-aperture size below 3 μm, we successfully developed and adopted a hybrid etch mask combining PR and SiNx for mesa etching. This hybrid mask enabled us to achieve nearly vertical etching sidewalls while effectively mitigating concerns about SiNx film stress. This technique significantly improved process controllability, oxidation uniformity, and reliability, addressing key challenges associated with the fabrication of small-aperture Cryo-VCSELs. The fabricated devices demonstrated excellent optical performance at cryogenic temperatures, achieving high output power and modulation bandwidth, making these devices promising candidates for next-generation optical data links in cryogenic and quantum computing systems. While this work focused on Cryo-VCSELs, the developed process is broadly applicable to various VCSEL designs requiring precise aperture control and uniformity. The hybrid mask technique provides a scalable and adaptable solution for high-performance VCSEL fabrication.

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Acronyms

VCSEL: Vertical Cavity Surface Emitting Laser
RT: Room Temperature
IR: Infrared
ICP-RIE: Inductively Coupled Plasma Reactive Ion Etch
BCB: Benzocyclobutene
SEM: Secondary Electron Microscopy
PR: Photoresist
PECVD: Plasma-Enhanced Chemical Vapor Deposition
DBR: Distributed Bragg Reflector
IQR: Interquartile Range
PAM-4: Pulse Amplitude Modulation with 4 levels
TDECQ: Transmitter and Dispersion Eye Closure Quaternary
FFE: Feed-Forward-Equalizer