LOL 1000 Liftoff Resist as an Antireflective Coating for MMIC Electroplating

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Abstract

This work demonstrates the use of Liftoff Layer (LOL) 1000 as an antireflective coating (ARC®) that reduces process variability and increases device yield. Using LOL 1000 resist as an ARC® layer, we have yielded 6 µm pads 7 µm apart. Replacing a standard ARC® eliminated an dry etch from the monolithic microwave integrated circuit (MMIC) air bridge process as well as reduced critical error-prone process steps leading to wafer-scale fabrication failure.

INTRODUCTION

Thick gold electroplating is an essential step in the fabrication of compound semiconductor devices due to the high current densities offered by the GaN high electron mobility transistor (HEMT) material system [1]. The process enables air bridges for multi-fingered devices. Air bridges are commonly found in compound semiconductor manufacturing, but are one of the more difficult processes in monolithic microwave integrated circuit (MMIC) fabrication due to several irreversible processing steps. An ARC® serves to reduce reflections from topography which can interfere with processing.

An antireflective coating (ARC®) is necessary in air bridge fabrication to reduce the lithography illumination reflecting off the sputtered gold seed layer and exposing the underside of the AZ® 15nXT resist. This leads to exposed AZ® 15nXT which blocks plating in that area. This compels us to use an ARC®. This paper explores the fabrication of air bridges without an ARC® and with the use of two separate ARCs®, XHRiC-16 and LOL 1000.

METHODS

Air bridges are fabricated as follows: 1) interconnect metal is evaporated, 2) a sacrificial 2.2 µm polymethylglutarimide (PMGI) (Kayakli Advanced Materials) *post* layer is patterned which defines contact to the bottom interconnect layer; 3) a sputtered Au layer of thickness 1500 Å is deposited which is used to seed electroplating; 4) an ARC® is used to reduce light scattering during the following *bridge* lithography step which defines the air bridges; 5) AZ® 15nXT negative photoresist is used to pattern *bridge;*.6) thick gold is electroplated to define the post and bridge structures.

DISCUSSION

Electroplating is the primary method of air bridge fabrication. This method is more cost-effective than sputtering or evaporating thick gold. AZ® 15 nXT (AZ Electronic Materials) is a thick negative resist generally used for defining bridge lithography for electroplating. Since there is a gold seed layer under the AZ® 15 nXT, the i-line exposure reflects off the seed layer, thus exposing the underside of the AZ® 15 nXT, as demonstrated in Figure 1 a) and Figure 1 b). This inadvertently exposed resist will not develop away and prevents plating on the gold metal pads.

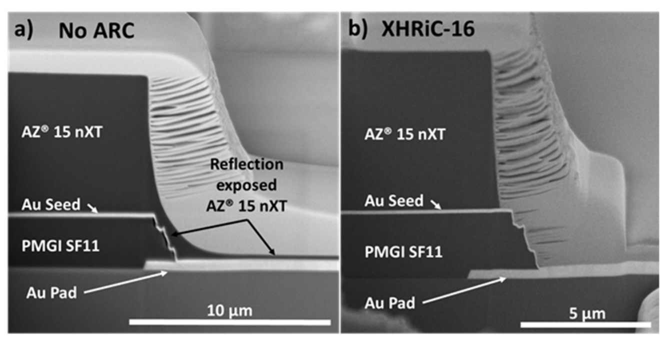

Figure 1 a) Cross-section of reflection exposed AZ® 15 nXT resist layer undeveloped on gold pads and b) cross-section of a straight sidewall profile using XHRiC-16.

XHRiC-16, manufactured by Brewer Sciences, was evaluated first. XHRiC-16 is able to absorb the reflected i-line exposure, so the underside of the AZ® 15 nXT remained un-exposed, as shown in Figure 1 b). XHRiC-16 requires a dry etch and is not affected during the AZ® 15 nXT develop process with AZ® 300 Metal Ion Free (MIF) (EMD Performance Materials). After wet-developing AZ® 15 nXT, the XHRiC-16 is removed with an O_2 reactive ion etch (RIE) which causes the gold seed layer to sputter onto the sidewalls of the AZ® 15 nXT as seen in Figure 2 a) and Figure 2 b).

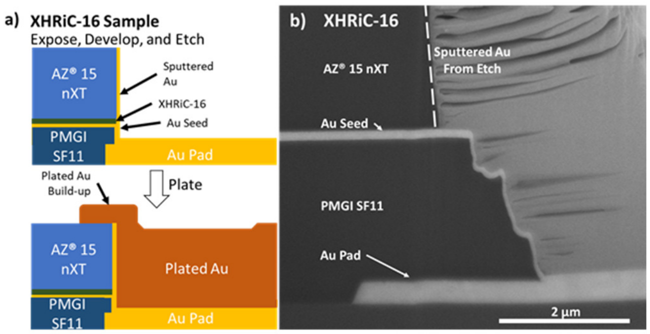

Figure 2 a) Schematic cross-section and process for plating a sample using XHRiC-16 and b) cross-section of sputtered gold along the sidewall after etching XHRiC-16.

The sputtered seed causes a conduction pathway during electroplating, which produces gold plating build-up on the edges of the structures. This plating build-up can cause tight geometries to become shorted to one another, demonstrated in Figure 3.

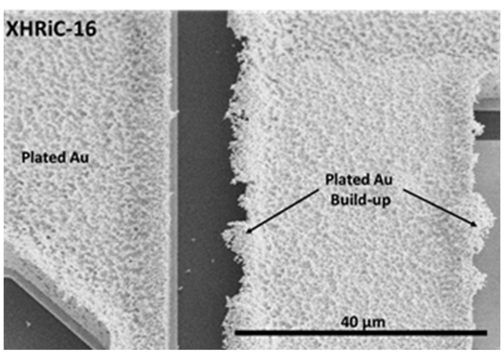

Figure 3 Top-down SEM of plated gold build-up from sidewall sputtered gold after etching XHRiC-16 as an ARC®.

After plating, the XHRiC-16 must be dry-etched again to expose interconnect metal for device testing. Ideally, ARC® can wet-develop concurrently with the AZ® 15 nXT process.

LOL 1000 (Dow), a liftoff resist, is also evaluated as an ARC®. During lithography, it absorbs reflected i-line illumination, which protects the underside of the AZ® 15 nXT from exposure, as seen in Figure 4 a). LOL 1000 is wet-developed concurrently with AZ® 15 nXT using AZ® 300MIF developer. This eliminates the dry etch requirement and prevents gold seed sputtering onto the AZ® 15 nXT sidewalls. The combination of LOL1000 and AZ® 15 nXT results in the best electroplating process for air bridges, as shown in Figure 4 b). LOL1000 has yielded tight geometries, such as 7 µm between 6 µm of plated gold on pads.

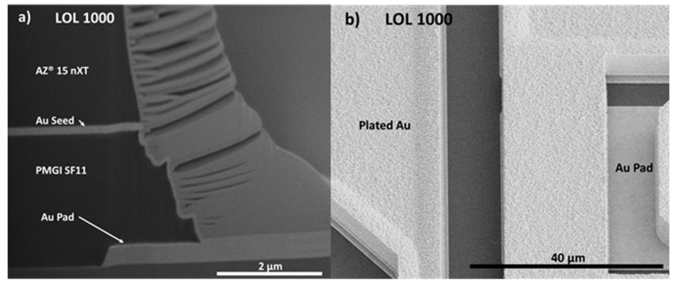

Figure 4 a) Cross-section of a clean AZ® 15 nXT sidewall profile after developing LOL 1000 and b) top-down SEM of clean plated gold after using LOL 1000 as an ARC®.

CONCLUSION

Using LOL 1000 resist as an ARC® layer, we have yielded tight geometries of 7 µm between 6 µm of plated gold on pads. Using this process, we have eliminated an RIE etch from the MMIC air bridge process as well as reduced critical error-prone process steps leading to wafer-scale fabrication failure.

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REFERENCES

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ACRONYMS

ARC®: Antireflective coating
HEMT: High electron mobility transistor
LOL: Liftoff layer
MIF: Metal ion free
MMIC: Monolithic microwave integrated circuit
PMGI: Polymethylglutarimide
RIE: Reactive ion etch