Low Off-State Leakage Current Normally Off p-GaN Gate HEMT Using the $Al_{0.5}Ga_{0.5}N$ Etching Stop Layer Design

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Keywords: p-GaN gate HEMT, normally off, etching stop layer, and high selection ratio

Abstract

In this work, normally off p-GaN/AlGaN/GaN high-electron-mobility transistors (HEMTs) were developed using $Al_{0.5}Ga_{0.5}N$ etching stop layer. Compared with AlN etching stop layer, the device not only decreased lattice defects but has also improved the linearity in drain current, which can be attributed to lattice matching. The results show that the $Al_{0.5}Ga_{0.5}N$ etching stop layer can reduce surface dislocation and obtain better characteristics. The p-GaN HMET using $Al_{0.5}Ga_{0.5}N$ etching stop layer achieved a higher drain current on/off ratio of 2.47×10^7, lower gate leakage current of 1.55×10^{-5} A/mm, and low on-state resistance of 21.65 Ω·mm. The dynamic R_{ON} of $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer device are 1.69 times and 2.26 times.

INTRODUCTION

Gallium nitride (GaN)-based high-electron-mobility transistors (HEMTs) show promising potential for high switching speed and high-power semiconductor device applications owing to their high electric field strength, high mobility, and good thermal stability [1]. Normally off behavior of AlGaN/GaN HEMTs with a sufficiently large and stable V_{TH} is highly desirable due to single voltage supply consideration. Thus, several researches have been proposed to realize the normally off operation characteristics of the AlGaN/GaN HEMTs, such as ultrathin barrier (UTB) [2], gate-recessed structures [3], [4], fluorine treatment [5], [6], and p-type gate. However, the structure with p-type gate has drawn increasing attention in the industry due to its low on-state resistance and large threshold voltage. Since the p-GaN gate etching process is a key factor in device processes, an appropriate etching depth control is strongly required. The residual p-GaN layer beyond the gate area depletes the 2DEG channel and causes a low forward current. Moreover, if the AlGaN barrier layer is etched in this step, the channel carrier density is decreased because of decreasing the spontaneous polarization. The techniques of $Al_{0.5}Ga_{0.5}N$ etching stop layer were researched. In addition to matching the lattice, the lattice defect is still decreased. In this work, an $Al_{0.5}Ga_{0.5}N$ etch stop layer was used between the p-GaN and AlGaN barrier and compared with AlN etching stop layer. Moreover, high-performance normally off p-GaN/AlGaN/GaN HEMTs have been realized.

EXPERIMENTAL PROCEDURES

In this work, the p-GaN/AlGaN/GaN HEMT was grown on 6-inch Si (111) substrates by MOCVD. Figure 1(a) shows the component structure, in which the active Mg concentration was $1\times10^{18}cm^{-3}$. For device fabrication, the active region was protected by photoresist, and the mesa-isolation region was etched to a depth of 200 nm in a reactive ion etching chamber using BCl_3/Cl_2 mixed gas plasma. A 5-μm-long p-type GaN gate finger was formed by etching using the p-GaN/$Al_{0.5}Ga_{0.5}N$ interface design. A mixture of $BCl_3/Cl_2/SF_6$ gas plasma was adopted to remove p-GaN for 120 s to form the gate terminals, with a resulting etching rate of 0.625nm/sec. The SF_6 plasma reacted with Al atoms and formed a thin AlF_3 etching stop layer when the mixed gas plasma reached the $Al_{0.5}Ga_{0.5}N$ barrier layer. As shown in Fig. 1(b), the p-GaN removal depth was measured using an atomic force microscope. To ensure uniform and complete removal of the p-GaN layer, a 240-s etch was used with 120-s over etching, and an obvious etching stop function was achieved by adopting $Al_{0.5}Ga_{0.5}N$ layer design [7]. Subsequently, the sample was immersed into diluted HF/NH_4OH chemical solution to remove the newly formed AlF_3 and AlO_x compounds. Ti/Al/Ni/Au (25/120/25/150nm) ohmic metal stack was then deposited as source and drain by electron beam evaporation (E-gun), and it was annealed at 875°C for 30 s in an N_2 atmosphere by RTA system. Third, the device was fabricated with implant isolation by oxygen implantation. Finally, the Ni/Au (25/120nm) gate electrode with the gate length of 2 μm was deposited by electron beam evaporation, and 100 nm of SiN was passivated.

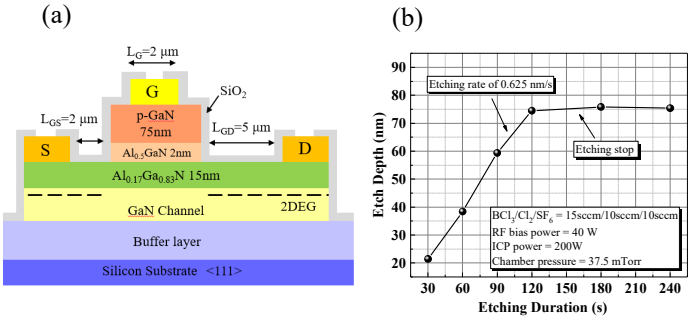

Fig.1. (a) Cross-sectional structure of the p-GaN gate HEMT and (b) p-GaN removal depth as a function of etch duration

RESULTS AND DISCUSSION

Figure 2 shows the X-ray diffraction (XRD) measurement. The full width at half maximum (FWHM) of the (002) symmetric reflection and the (102) asymmetric reflection was taken as a measure of crystalline quality. In this work, we measured the surface of the device, mainly analyzing the crystal quality of the surface. The (002) rocking curve scan yields information about the extent of tilt with respect to the surface of the device, and its FWHM is a qualitative measure of the screw dislocation density (N_{screw}) [8]. The (102) scan yields twist with respect to the surface of the device, and its FWHM is measure of edge dislocation density (N_{edge}). After calculation, the total dislocation (N_{total}) using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer is 2.23×10^{8} and 3.57×10^{8}per cm^{-2}, respectively. As shown in Fig. 2, the screw dislocation density and edge dislocation density are lower in case of using $Al_{0.5}Ga_{0.5}N$ etching stop layer.

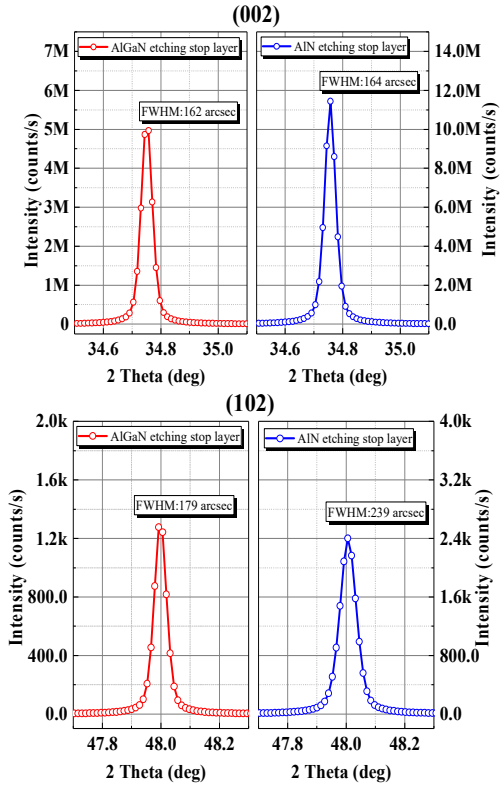

Fig.2. XRD measurement—the full width at half maximum (FWHM) of the (002) symmetric reflection and the (102) asymmetric reflection using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer

Figure 3(a) and (b) shows the log-scale transfer (I_{DS}–V_{GS}) and output (I_{DS}–V_{DS}) characteristics using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer. As shown in Fig. 3(a), the off-state current for using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer was 4.11×10^{-6} and 4.31×10^{-5} mA/mm, respectively. This implies that using $Al_{0.5}Ga_{0.5}N$ etching stop layer results in lower trap density in the device channel. By contrast, lower aluminum mole fraction in etching stop layer can decrease the trap density of channel and can cause lattice matching. Additionally, the maximum output current density (I_{Dmax}) was 121 and 67 mA/mm at a gate bias of 4V, respectively. The I_{Dmax} value using $Al_{0.5}Ga_{0.5}N$ etching stop layer was 43% higher than that of using AlN etching stop layer due to the suppressed trap density of channel.

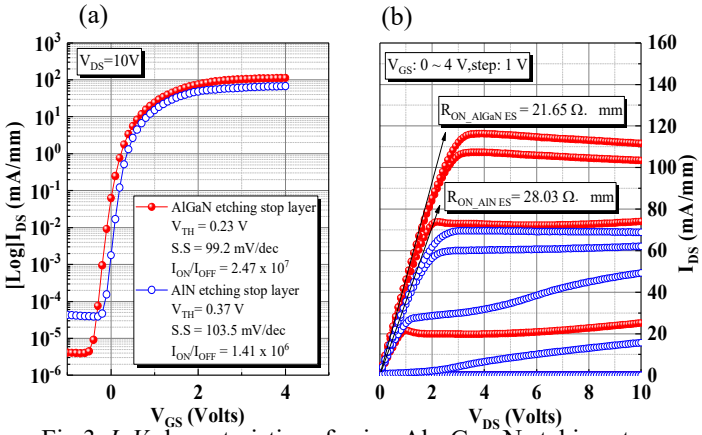

Fig.3. *I–V* characteristics of using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer with $L_{GS}/L_G/L_{GD}/W_G$ = 2/2/5/100 μm, (a) transfer characteristic, and (b) output characteristic

Figure 4(a) shows the gate leakage current I_{GS} of a 2-μm gate device. Clearly, using $Al_{0.5}Ga_{0.5}N$ etching stop layer exhibits better gate leakage than AlN etching stop layer, with a gate leakage improvement from 9.27×10^{-5} to 1.55×10^{-5} at a gate bias of −10V. After calculation, the static on-resistance using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer is 21.65 and 28.03Ω·mm, respectively, corresponding to a specific on-resistance (R_{sp}) of 2.59 and 3.36 m Ω·cm^2. The off-state breakdown voltage using $Al_{0.5}Ga_{0.5}N$ etching stop layer and AlN etching stop layer was 561V and 501V at V_{GS} = −1V, and FOM was 83.11 and 44.37MW/cm^2, respectively, as shown in Fig4(b).

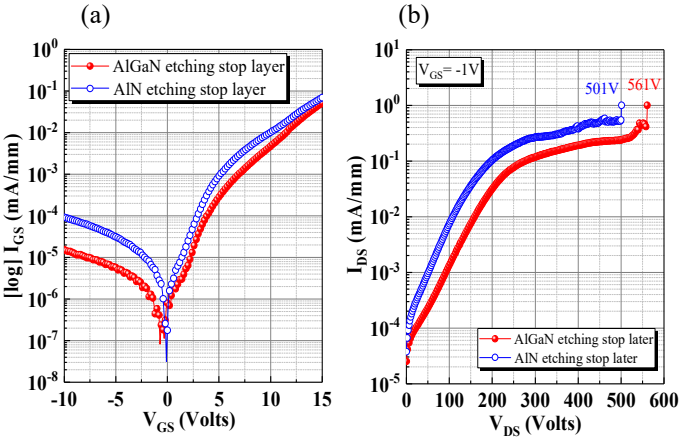

Fig.4. (a) Gate leakage characteristics and (b) off-state breakdown voltage measurement

As shown in Fig. 5, the I_{DS}–V_{DS} pulsed characteristic was also measured from different quiescent bias points at V_{GS} = 4 V to investigate the influence of off-state gate bias stress on dynamic R_{ON} and I_{DS}. The reference off-state was set as (V_{GSQ}, V_{DSQ}) = (0 V, 0 V), which does not induce any relevant trapping. The device is switched with 2-µs pulse width and 200-µs period, respectively. The quiescent gate bias (V_{GSQ}) was swept from 0 to −3 V. Apparently, the current collapse of the AlN etching stop layer device is worse than that of the $Al_{0.5}Ga_{0.5}N$ etching stop layer device, and the high gate lag of the AlN etching stop layer device under relatively gate voltage stress results in I–V slope decreases, indicating that its surface defect trap density is higher than that of the $Al_{0.5}Ga_{0.5}N$ etching stop layer device. The dynamic R_{ON} ($R_{ON}/R_{ON(0,0)}$) of the $Al_{0.5}Ga_{0.5}N$ etching stop layer device slightly increased with higher gate bias stress from 0 to −3 V due to low electron injection into the surface trap states from the gate electrode, and the dynamic R_{ON} ratio increased to 2.26 at the off-state gate bias stress of −3 V for the AlN etching stop layer device.

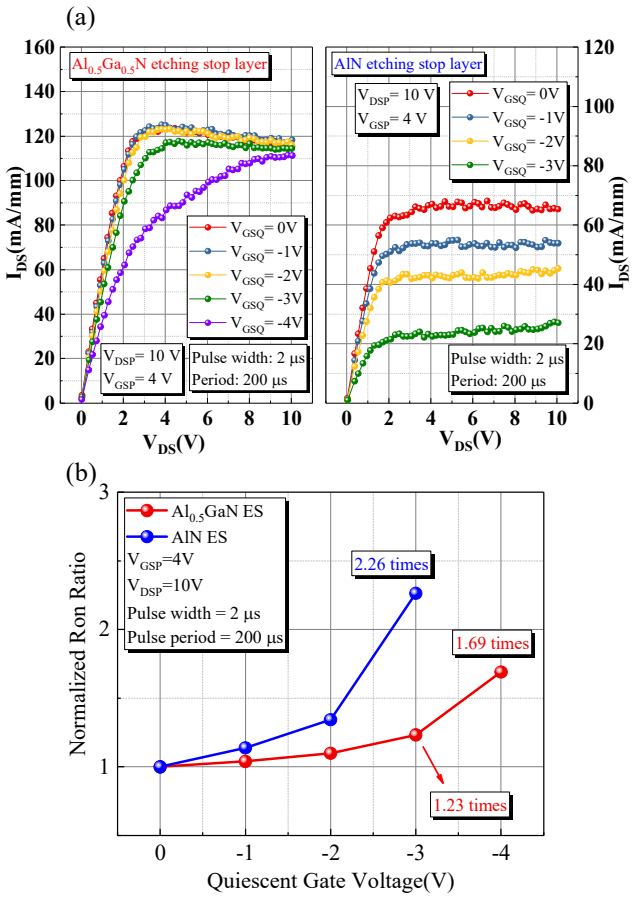

Fig.5. (a) Pulsed I_{DS}–V_{DS} characteristics from quiescent gate bias point of 0 V to an on-state at 4 V with 2-µs pulse width and 200-µs pulse period—afterward, the quiescent gate bias (V_{GSQ}) was swept from 0 to −3 V and (b) dependence of the R_{ON} collapse ratio versus quiescent gate voltage

CONCLUSIONS

In this work, $Al_{0.5}Ga_{0.5}N$ etching stop layer was applied for p-GaN/AlGaN/GaN HEMT. The dislocation density was clearly proved after XRD measurement. Using $Al_{0.5}Ga_{0.5}N$ etching stop layer exhibited lower dislocation density, lower off-state current, lower gate leakage, lower on-resistance, higher on/off ratio, and higher off-state breakdown voltage. The dynamic R_{ON} of $Al_{0.5}GaN$ etching stop and AlN etching stop device are 1.23 times and 2.26 times at the off-state gate bias stress of −3 V, respectively. Using $Al_{0.5}Ga_{0.5}N$ etching stop layer can match the lattice and improve the ratio of dynamic resistance. Therefore, using $Al_{0.5}Ga_{0.5}N$ etching stop layer is a promising method for fabricating high-performance normally off p-GaN HEMTs.

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